

DELL/COMPAL

MODEL NAME : FDV42

PCB NO : LA-J272P

BOM P/N :

GPIO MAP: X11\_CMLH\_GPIO map Rev0.4\_20190927

PWR Circuit : BHMLK\_CMLH\_14DSC\_X01\_PWR\_20191022C

## Brook Hollow MLK 14 DSC (TBT)

Comet Lake H

2019-10-24

REV : 0.2 (X01)

X76@ :  
2GSAMX76@  
2GMICRX76@  
2GHYNX76@

@ : Nopop Component  
EMI@ : EMI Component  
@EMI@ : EMI Nopop Component  
ESD@ : ESD Component  
@ESD@ : ESD Nopop Component  
RF@ : RF Component  
@RF@ : RF Nopop Component  
VPRO@ : VPRO support  
NVPRO@ : non VPRO support  
JUMP@ : Jump solder and short  
@JUMP@ : Jump no solder  
XDP@ : XDP Component  
@XDP@  
CONN@ : Connector Component  
WWAN@ : WWAN Component  
WWANRF@ : WWAN RF Component

ESPI@ : eSPI interface  
DS3@ : Deep sleep support  
NDS3@ : non Deep sleep support  
@NDS3@ : non Deep sleep Nopop Component  
RTD3@ : RTD3 support  
NRTD3@ : non RTD3 support  
5107ES@ :  
5107NES@ :  
2GSAM@  
2GMICR@  
2GHYN@

MB PCB

Part Number	Description
DAB00063000	PCB 2VW LA-J272P REV0 M/B 1 S

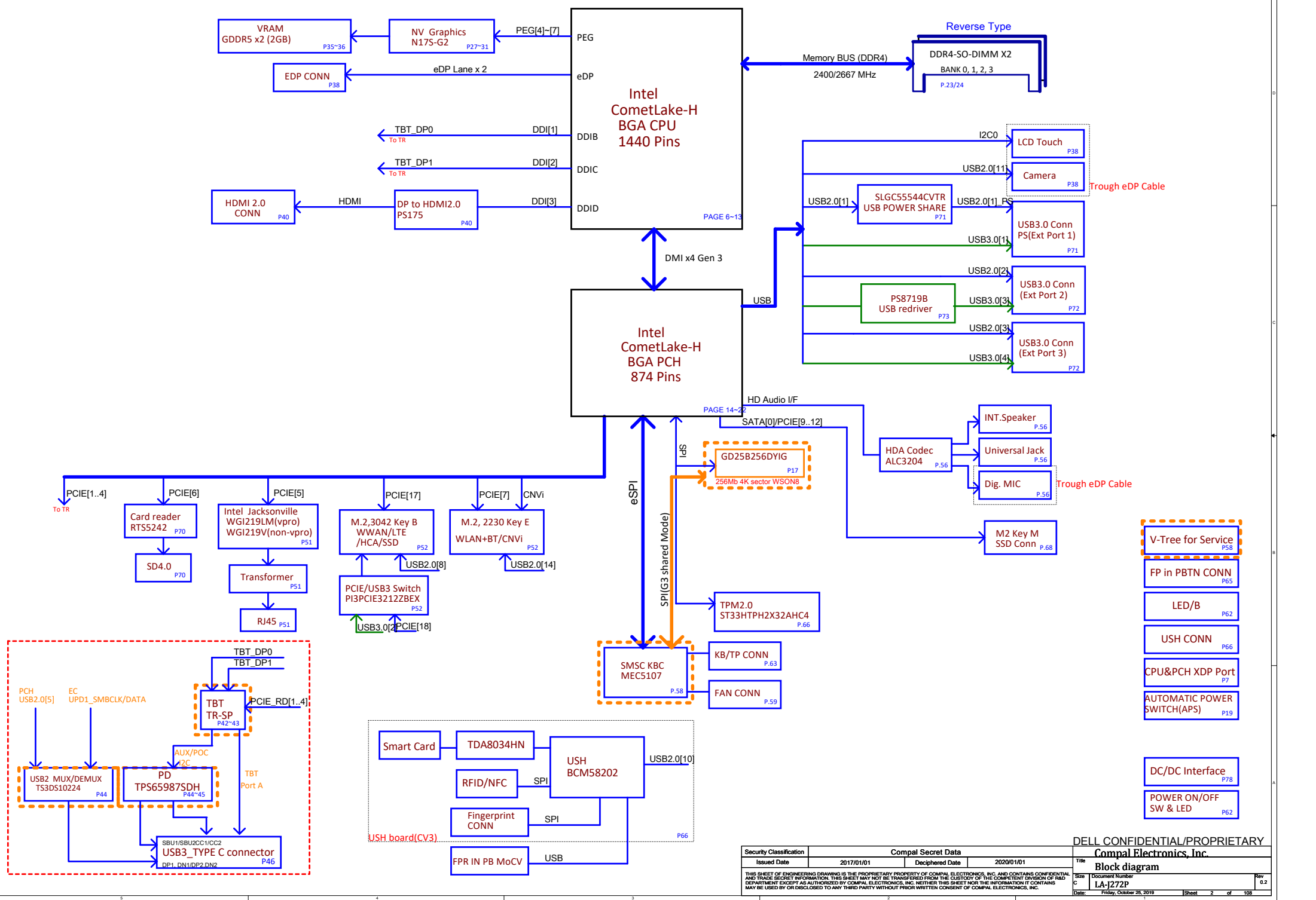
Layout Dell logo



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REV:X00  
PWB:

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Brook Hollow MLK 14 DSC TBT Block Diagram



POWER STATES

Signal State	SLP S3#	SLP S4#	SLP S5#	SLP A#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

power plane State	+5V_ALW +3.3V_ALW +3.3V_ALW_DSW +3.3V_ALW_PCH +RTC_CELL +1.8V_PRIM +1.0V_PRIM +1.0V_PRIM_CORE +5V_ALW2 +3.3V_ALW2 +3.3V_RTC_LDO +1.0V_MPHYGT	+3.3V_SUS +1.2V_MEM +1.0V_VCCST +2.5V_MEM	+5V_RUN +3.3V_RUN +0.6V_DDR_VTT +1.2V_RUN +VCC_CORE +VCC_GT +1.0VS_VCCIO +VCC_SA +1.8V_RUN
S0	ON	ON	ON
S3	ON	ON	OFF
S5 S4/AC	ON	OFF	OFF
S5 S4/AC doesn't exist	OFF	OFF	OFF

Layer No.	Name	Er	Material	Thickness (Material SPEC.) Unit - mil	Thickness (Actuality) Unit - mil
			SolderMask	Material: IT-158	0.50
			Add Plating		
1	Top	3.7	Copper foil	0.5oz/plating	1.60
2	GND/VCC	3.9	Copper foil	0.5 oz	3.27
3	IN 1	3.9	Copper foil	3mil	0.60
4	IN 2	3.9	Copper foil	0.5 oz	0.60
5	GND/VCC	3.9	Copper foil	3mil	0.60
6	IN 3	3.9	Copper foil	0.5 oz	0.60
7	IN 4	3.9	Copper foil	3mil	0.60
8	GND/VCC	3.9	Copper foil	0.5 oz	0.60
9	IN 5	3.9	Copper foil	3mil	0.60
10	IN 6	3.9	Copper foil	0.5 oz	0.60
11	GND/VCC	3.7	Copper foil	0.5 oz	3.00
12	Bottom	3.7	Copper foil	0.5 oz	3.27
			Add Plating		
			SolderMask	Material: 0.5oz/plating	1.60
					0.50
Overall Thickness (1.2mm ± 10%)					47.19
					19634

Figure 110. High Speed I/O (HSIO) Lane Multiplexing in PCH-H

Flex I/O Lane	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
High Speed I/O (HSIO) Type and Lane	USB3.1 Gen1/Gen2 #1	USB3.1 Gen1/Gen2 #2	USB3.1 Gen1/Gen2 #3	USB3.1 Gen1/Gen2 #4	USB3.1 Gen1/Gen2 #5	USB3.1 Gen1/Gen2 #6	USB3.1 Gen1/Gen2 #7	PCIE #1	PCIE #2	PCIE #3	PCIE #4	PCIE #5	PCIE #6	PCIE #7	PCIE #8	PCIE #9	PCIE #10	PCIE #11	PCIE #12
Intel® RSF Support								No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support

USB3.0	SSIC	PCIE	SATA	DESTINATION
USB3.0-1				JUSB1-->Right
USB3.0-2	SSIC-1			JNGFF2-->M2 3042(LTE)
USB3.0-3	SSIC-2			JUSB2-->LEFT
USB3.0-4				JUSB3-->RIGHT
USB3.0-5				NA
USB3.0-6				NA
USB3.0-7		PCIE-1		Titan Ridge - SP
USB3.0-8		PCIE-2		
USB3.0-9		PCIE-3		
USB3.0-10		PCIE-4		
		PCIE-5		LOM
		PCIE-6		Card Reader
		PCIE-7		JNGFF1-->M.2 2230(WLAN)
		PCIE-8		NA
		PCIE-9		M.2 Socket 3 (Key M) M.2 2280 SSD (PClex4 or SATA)
		PCIE-10	SATA-0A	
		PCIE-11	SATA-1A	
		PCIE-12	SATA-1A	
		PCIE-13	SATA-0B	NA
		PCIE-14	SATA-1B	NA
		PCIE-15	SATA-2	NA
		PCIE-16	SATA-3	NA
		PCIE-17	SATA-4	M.2 3042 (HCA or QCA LTE) SSD Cache
		PCIE-18	SATA-5	
		PCIE-19	SATA-6	NA
		PCIE-20	SATA-7	NA

USB PORT#	DESTINATION
1	JUSB1-->Right
2	JUSB2 ->LEFT
3	JUSB3-->RIGHT
4	FP IN PB
5	TI PD
6	test point
7	NA
8	JNGFF2-->M2 3042(WWAN)
9	NA
10	JUSH1-->USH
11	JEDP1-->Camera
12	NA
13	NA
14	JNGFF1--> M.2 2230(CNVi_BT)

USH	H	BIO
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VIDEO	DESTINATION
eDP	LCD
DDI-B	Titan Ridge - SP (Port 0)
DDI-C	Titan Ridge - SP (Port 1)
DDI-D	PS175 --> JHDMI1

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Port Assignment

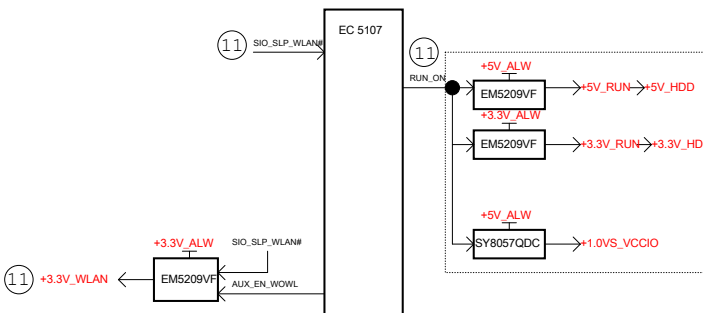
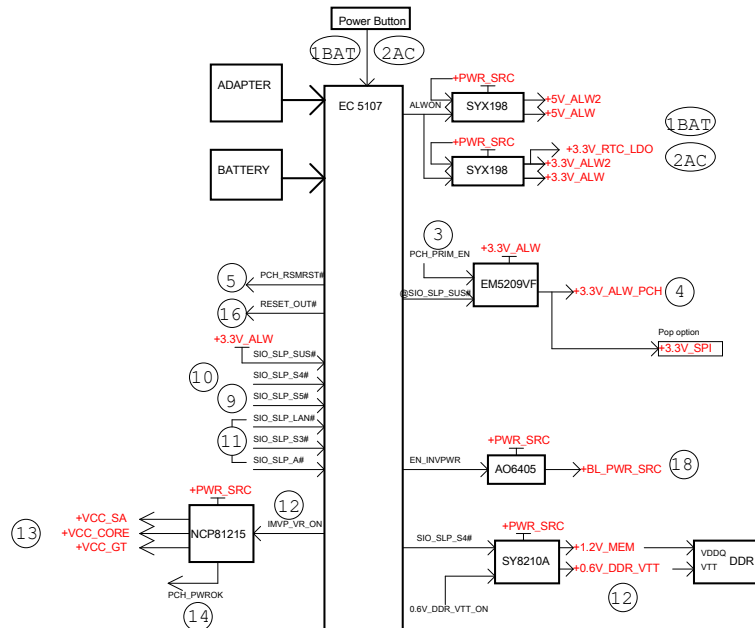
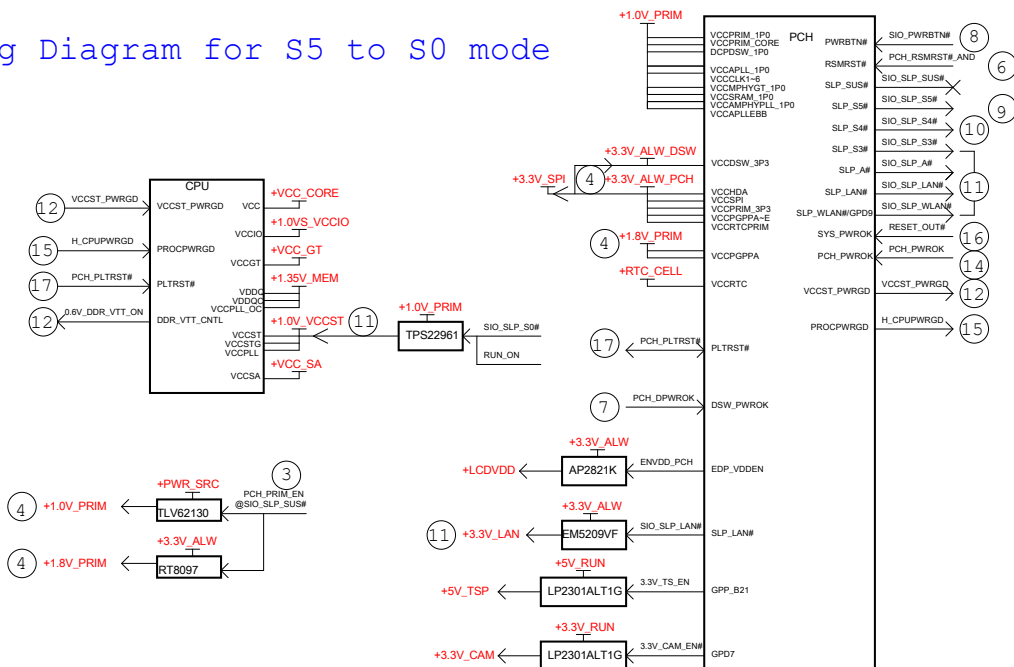
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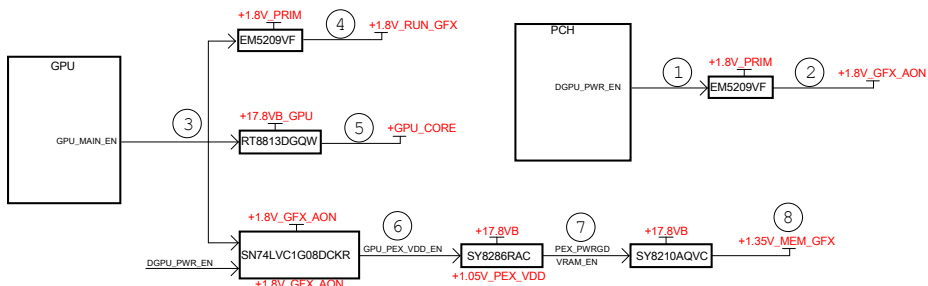
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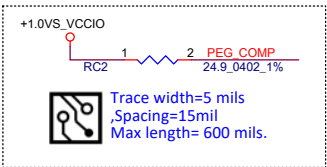
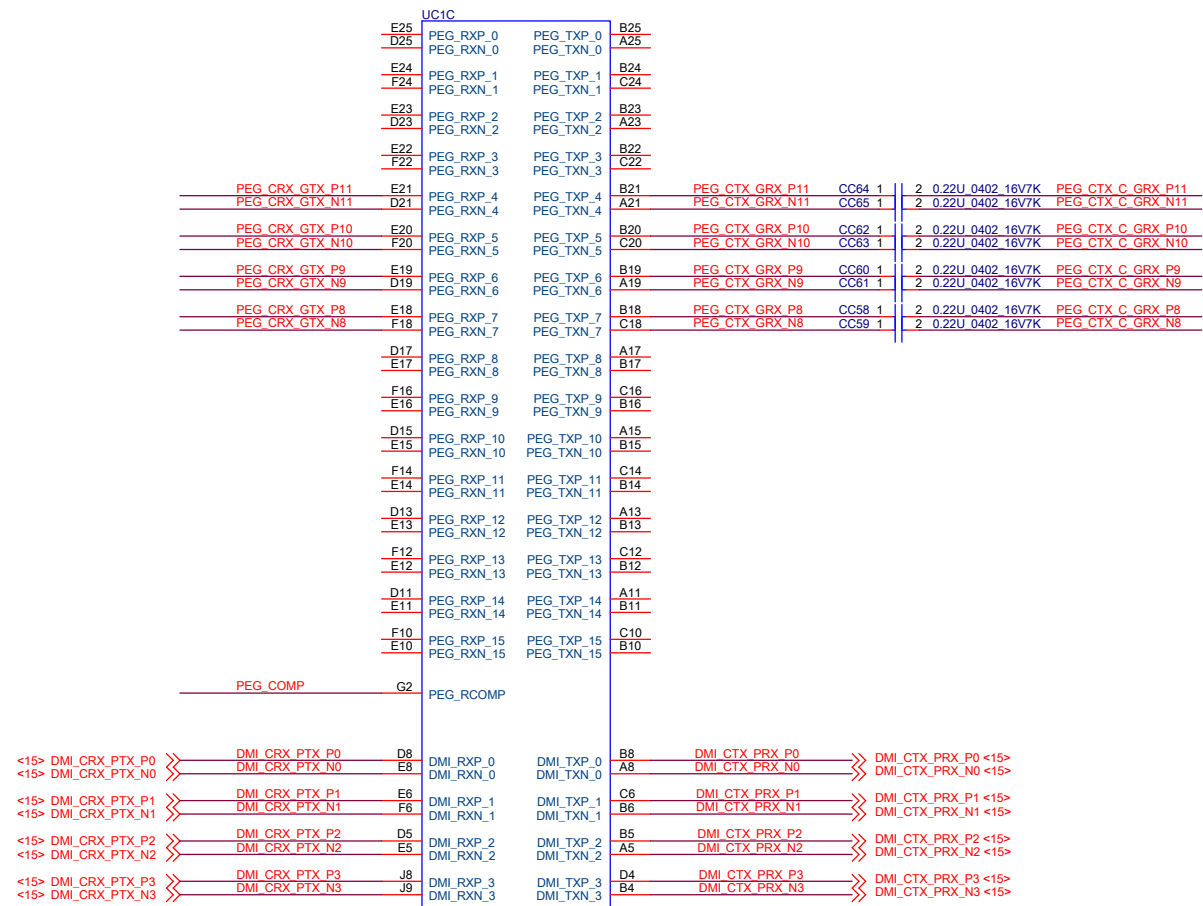
### Timing Diagram for S5 to S0 mode

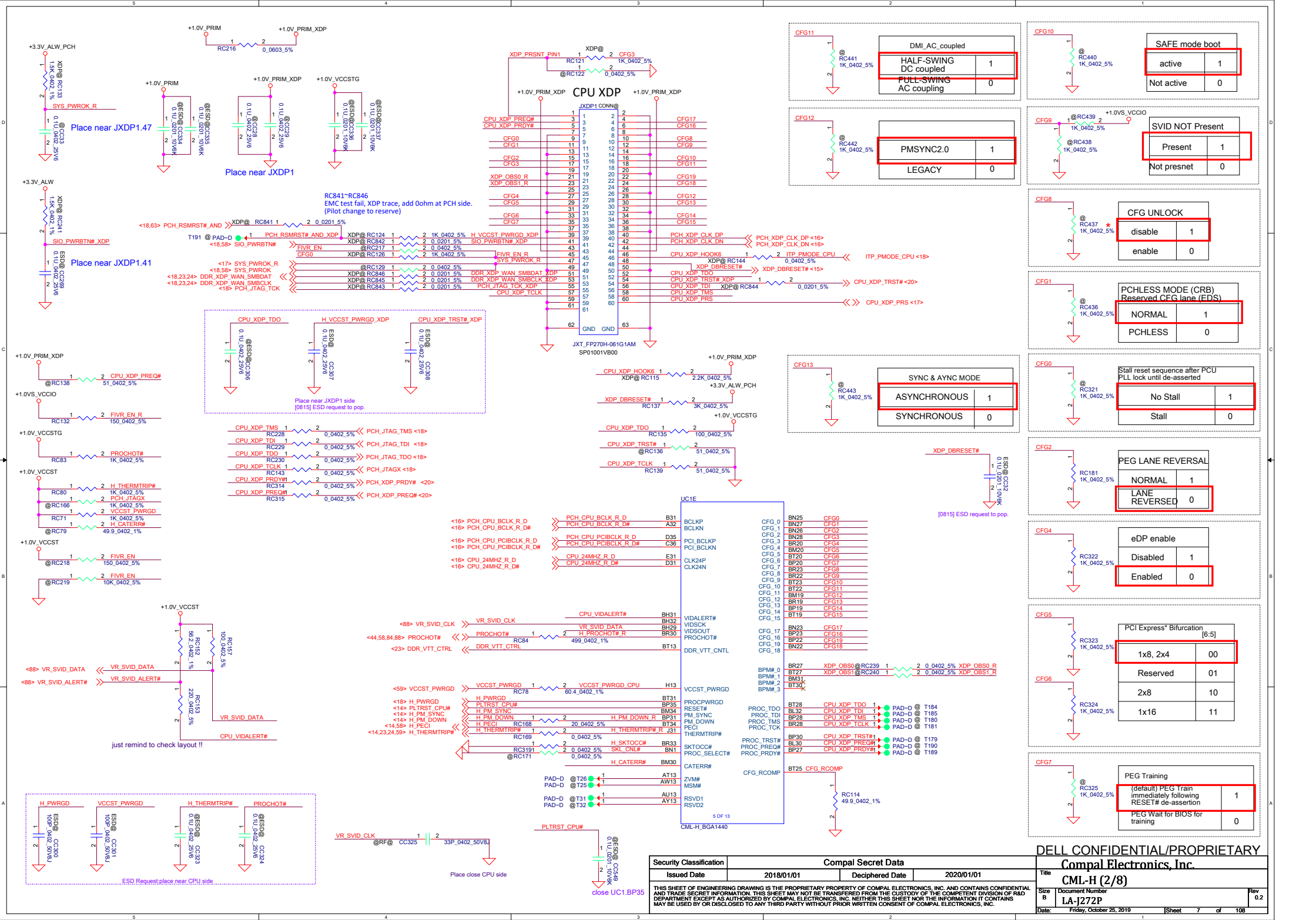


## GPU power-on Timing Diagram during win10

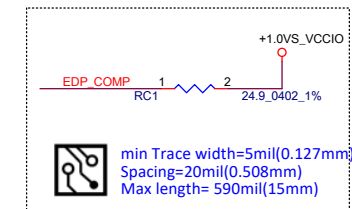
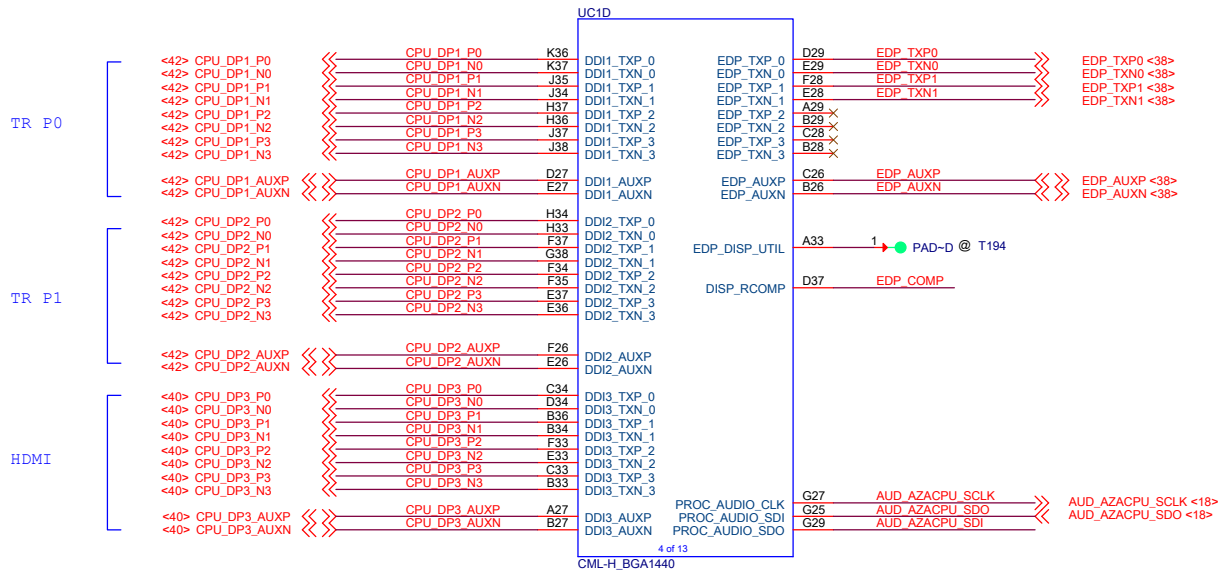


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PEG CRX GTX N[8..11] << PEG\_CRX\_GTX\_N[8..11] <27>  
PEG CTX C GRX P[8..11] >> PEG\_CTX\_C\_GRX\_P[8..11] <27>  
PEG CTX C GRX N[8..11] >> PEG\_CTX\_C\_GRX\_N[8..11] <27>

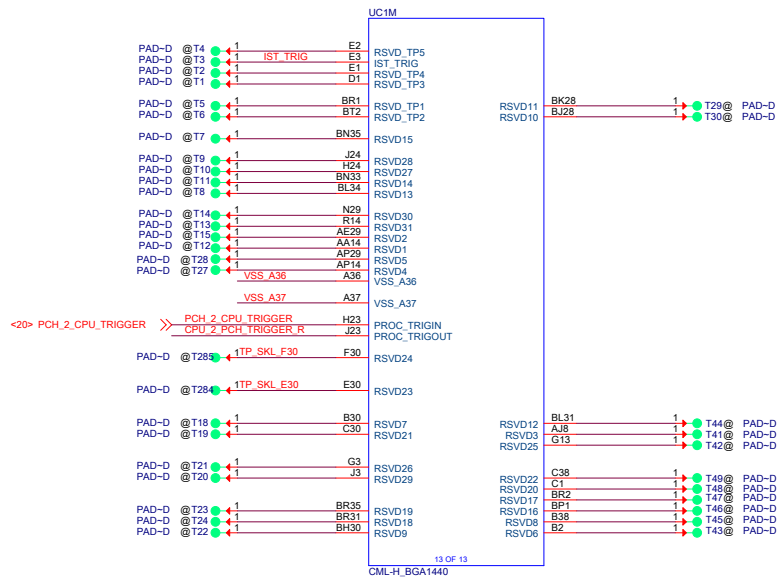




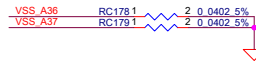




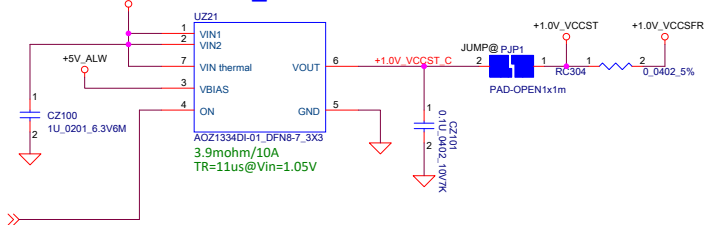
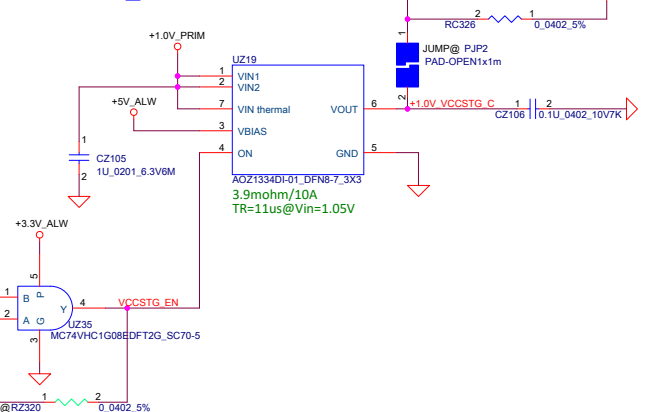
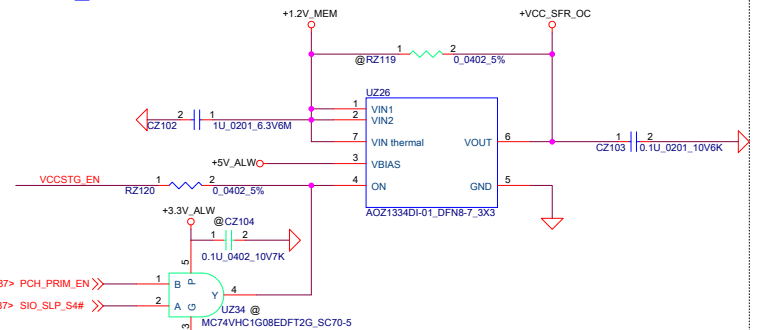
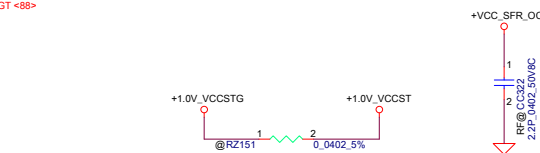
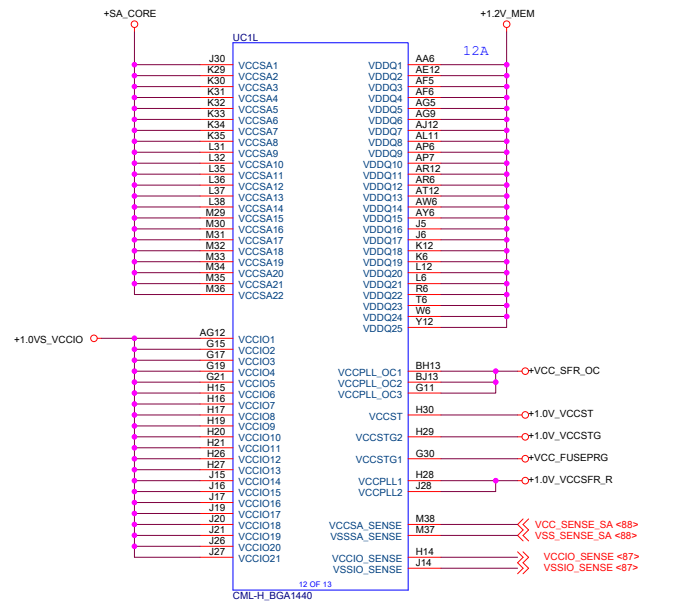
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<20> CPU\_2\_PCH\_TRIGGER << CPU\_2\_PCH\_TRIGGER 1 RC177 2 CPU\_2\_PCH\_TRIGGER R 30\_0402\_5%

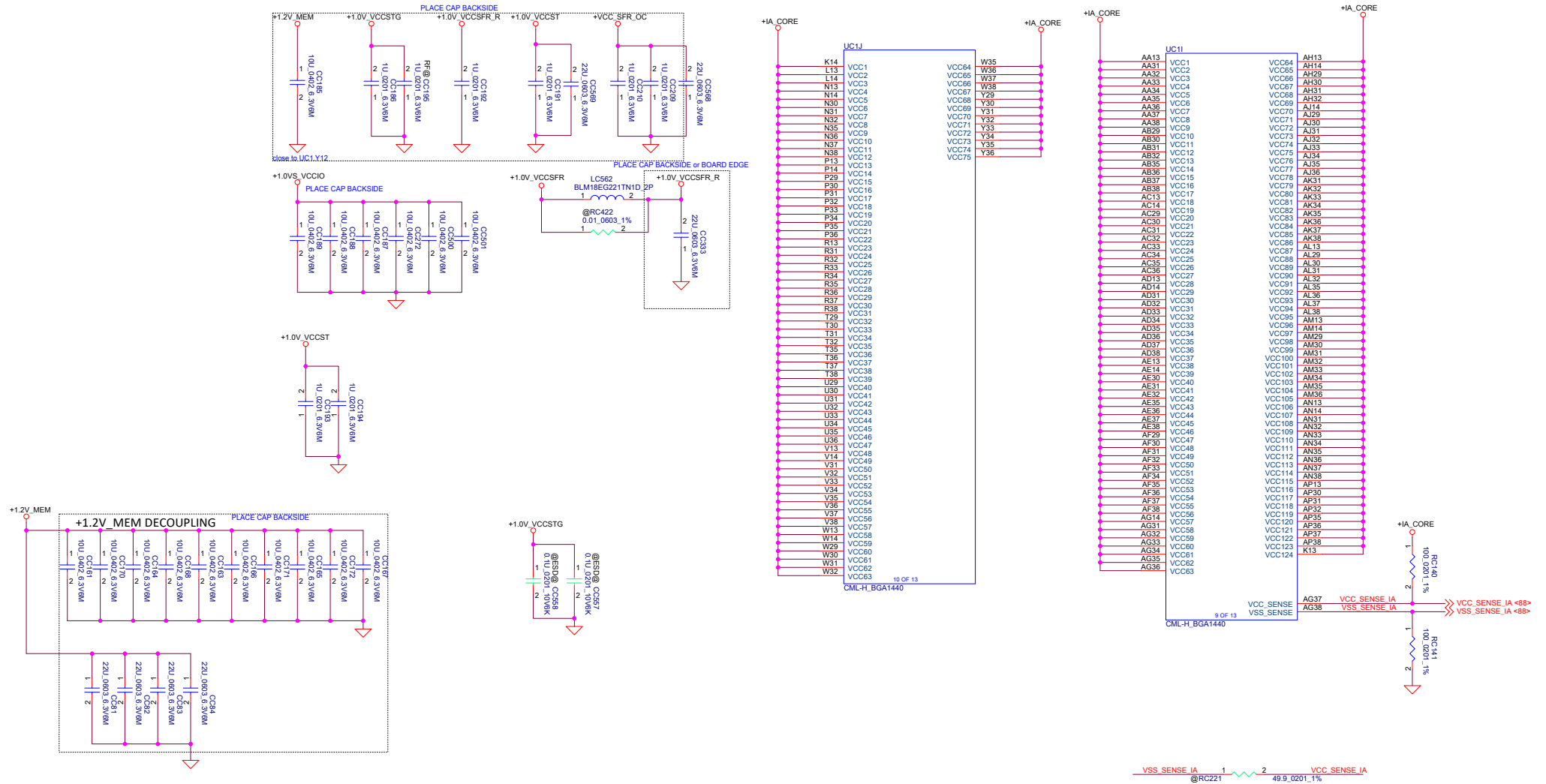


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CPU Decoupling CAP Follow 611586\_CML\_H\_PDG\_Rev0p7  
page. 592 ,593 Table 326. CML H 8+2 Processor Decoupling Requirements



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UC1F			AK4		
A10	VSS_1	VSS_82	AL10		
A12	VSS_2	VSS_83	AL12		
A16	VSS_3	VSS_84	AL14		
A18	VSS_4	VSS_85	AL33		
A20	VSS_5	VSS_86	AL34		
A22	VSS_6	VSS_87	AL4		
A24	VSS_7	VSS_88	AL7		
A26	VSS_8	VSS_89	AL9		
A28	VSS_9	VSS_90	AM1		
A30	VSS_10	VSS_91	AM12		
A6	VSS_11	VSS_92	AM2		
A9	VSS_12	VSS_93	AM3		
AA12	VSS_13	VSS_94	AM37		
AA29	VSS_14	VSS_95	AM38		
AA30	VSS_15	VSS_96	AM4		
AB33	VSS_16	VSS_97	AM5		
AB34	VSS_17	VSS_98	AN12		
AB6	VSS_18	VSS_99	AN29		
AC1	VSS_19	VSS_100	AN30		
AC12	VSS_20	VSS_101	AN5		
AC2	VSS_21	VSS_102	AN6		
AC3	VSS_22	VSS_103	AP10		
AC37	VSS_23	VSS_104	AP11		
AC38	VSS_24	VSS_105	AP12		
AC4	VSS_25	VSS_106	AP33		
AC5	VSS_26	VSS_107	AP34		
AC6	VSS_27	VSS_108	AP8		
AD10	VSS_28	VSS_109	AP9		
AD11	VSS_29	VSS_110	AR1		
AD12	VSS_30	VSS_111	AR13		
AD29	VSS_31	VSS_112	AR14		
AD30	VSS_32	VSS_113	AR2		
AD6	VSS_33	VSS_114	AR29		
AD8	VSS_34	VSS_115	AR3		
AD9	VSS_35	VSS_116	AR30		
AE33	VSS_36	VSS_117	AR31		
AE34	VSS_37	VSS_118	AR32		
AE6	VSS_38	VSS_119	AR33		
AF1	VSS_39	VSS_120	AR34		
AF12	VSS_40	VSS_121	AR35		
AF13	VSS_41	VSS_122	AR36		
AF14	VSS_42	VSS_123	AR37		
AF2	VSS_43	VSS_124	AR38		
AF3	VSS_44	VSS_125	AR4		
AF4	VSS_45	VSS_126	AR5		
AG10	VSS_46	VSS_127	AT29		
AG11	VSS_47	VSS_128	AT30		
AG13	VSS_48	VSS_129	AT6		
AG29	VSS_49	VSS_130	AU10		
AG30	VSS_50	VSS_131	AU11		
AG6	VSS_51	VSS_132	AU12		
AG7	VSS_52	VSS_133	AU33		
AG8	VSS_53	VSS_134	AU34		
AH12	VSS_54	VSS_135	AU6		
AH33	VSS_55	VSS_136	AU7		
AH34	VSS_56	VSS_137	AU8		
AH35	VSS_57	VSS_138	AU9		
AH36	VSS_58	VSS_139	AV38		
AH6	VSS_59	VSS_140	AW1		
AJ1	VSS_60	VSS_141	AW12		
AJ13	VSS_61	VSS_142	AW2		
AJ2	VSS_62	VSS_143	AW29		
AJ3	VSS_63	VSS_144	AW3		
AJ37	VSS_64	VSS_145	AW30		
AJ38	VSS_65	VSS_146	AW4		
AJ4	VSS_66	VSS_147	U6		
AJ5	VSS_67	VSS_148	V12		
AJ6	VSS_68	VSS_149	V29		
W4	VSS_69	VSS_150	V30		
W5	VSS_70	VSS_151	A14		
Y10	VSS_71	VSS_152	AD7		
Y11	VSS_72	VSS_153	V6		
Y13	VSS_73	VSS_154	W1		
Y14	VSS_74	VSS_155	W12		
Y37	VSS_75	VSS_156	W2		
Y38	VSS_76	VSS_157	W3		
Y7	VSS_77	VSS_158	W33		
Y8	VSS_78	VSS_159	W34		
Y9	VSS_79	VSS_160			
AK28	VSS_80	VSS_161			
AK30	VSS_81	VSS_162			

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UC1G			BJ15		
AW5	VSS_163	VSS_244	BJ15		
AY12	VSS_164	VSS_245	BJ18		
AY33	VSS_165	VSS_246	BJ22		
AY34	VSS_166	VSS_247	BJ25		
B9	VSS_167	VSS_248	BJ29		
BA10	VSS_168	VSS_249	BJ30		
BA11	VSS_169	VSS_250	BJ31		
BA12	VSS_170	VSS_251	BJ32		
BA37	VSS_171	VSS_252	BJ33		
BA38	VSS_172	VSS_253	BJ34		
BA6	VSS_173	VSS_254	BJ35		
BA7	VSS_174	VSS_255	BJ36		
BA8	VSS_175	VSS_256	BK13		
BA9	VSS_176	VSS_257	BK14		
BB1	VSS_177	VSS_258	BK15		
BB12	VSS_178	VSS_259	BK18		
BB2	VSS_179	VSS_260	BK22		
BB29	VSS_180	VSS_261	BK29		
BB3	VSS_181	VSS_262	BK6		
BB30	VSS_182	VSS_263	BL13		
BB4	VSS_183	VSS_264	BL14		
BB5	VSS_184	VSS_265	BL18		
BB6	VSS_185	VSS_266	BL19		
BC12	VSS_186	VSS_267	BL20		
BC13	VSS_187	VSS_268	BL21		
BC14	VSS_188	VSS_269	BL22		
BC33	VSS_189	VSS_270	BL29		
BC34	VSS_190	VSS_271	BL33		
BC6	VSS_191	VSS_272	BL35		
BD10	VSS_192	VSS_273	BL38		
BD11	VSS_193	VSS_274	BL6		
BD12	VSS_194	VSS_275	BM11		
BD37	VSS_195	VSS_276	BM12		
BD6	VSS_196	VSS_277	BM13		
BD7	VSS_197	VSS_278	BM14		
BD8	VSS_198	VSS_279	BM18		
BD9	VSS_199	VSS_280	BM2		
BE1	VSS_200	VSS_281	BM21		
BE2	VSS_201	VSS_282	BM22		
BE29	VSS_202	VSS_283	BM23		
BE3	VSS_203	VSS_284	BM24		
BE30	VSS_204	VSS_285	BM25		
BE4	VSS_205	VSS_286	BM26		
BE5	VSS_206	VSS_287	BM27		
BE6	VSS_207	VSS_288	BM28		
BF12	VSS_208	VSS_289	BM29		
BF33	VSS_209	VSS_290	BM3		
BF34	VSS_210	VSS_291	BM33		
BF6	VSS_211	VSS_292	BM35		
BG12	VSS_212	VSS_293	BM38		
BG13	VSS_213	VSS_294	BM5		
BG14	VSS_214	VSS_295	BM6		
BG37	VSS_215	VSS_296	BM7		
BG38	VSS_216	VSS_297	BM8		
BG6	VSS_217	VSS_298	BM9		
BH1	VSS_218	VSS_299	BN12		
BH10	VSS_219	VSS_300	BN14		
BH11	VSS_220	VSS_301	BN18		
BH12	VSS_221	VSS_302	BN19		
BH14	VSS_222	VSS_303	BN2		
BH2	VSS_223	VSS_304	BN20		
BH3	VSS_224	VSS_305	BN21		
BH4	VSS_225	VSS_306	BN24		
BH5	VSS_226	VSS_307	BN29		
BH6	VSS_227	VSS_308	BN30		
BH7	VSS_228	VSS_309	BN31		
BH8	VSS_229	VSS_310	BN34		
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T2	VSS_231	VSS_312	P6		
T3	VSS_232	VSS_313	R12		
T34	VSS_233	VSS_314	R29		
T4	VSS_234	VSS_315	AY14		
AD7	VSS_235	VSS_316	BD38		
T5	VSS_236	VSS_317	R30		
T7	VSS_237	VSS_318	T1		
T8	VSS_238	VSS_319	T10		
T9	VSS_239	VSS_320	T11		
U37	VSS_240	VSS_321	T12		
U38	VSS_241	VSS_322	T13		
BJ12	VSS_242	VSS_323	T14		
BJ14	VSS_243	VSS_324			

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UC1H			F15		
BN4	VSS_325	VSS_409	F15		
BN7	VSS_326	VSS_410	F17		
BP12	VSS_327	VSS_411	F19		
BP14	VSS_328	VSS_412	F2		
BP18	VSS_329	VSS_413	F21		
BP21	VSS_330	VSS_414	F23		
BP24	VSS_331	VSS_415	F25		
BP25	VSS_332	VSS_416	F27		
BP26	VSS_333	VSS_417	F3		
BP29	VSS_334	VSS_418	F31		
BP33	VSS_335	VSS_419	F36		
BP34	VSS_336	VSS_420	F4		
BP7	VSS_337	VSS_421	F5		
BR12	VSS_338	VSS_422	F8		
BR14	VSS_339	VSS_423	F9		
BR18	VSS_340	VSS_424	G10		
BR21	VSS_341	VSS_425	G12		
BR24	VSS_342	VSS_426	G14		
BR25	VSS_343	VSS_427	G16		
BR26	VSS_344	VSS_428	G18		
BR29	VSS_345	VSS_429	G20		
BR34	VSS_346	VSS_430	G22		
BR36	VSS_347	VSS_431	G23		
BR7	VSS_348	VSS_432	G24		
BT12	VSS_349	VSS_433	G26		
BT14	VSS_350	VSS_434	G4		
BT18	VSS_351	VSS_435	G5		
BT21	VSS_352	VSS_436	G6		
BT24	VSS_353	VSS_437	G8		
BT26	VSS_354	VSS_438	G9		
BT29	VSS_355	VSS_439	H11		
BT32	VSS_356	VSS_440	H12		
BT5	VSS_357	VSS_441	H18		
C11	VSS_358	VSS_442	H22		
C13	VSS_359	VSS_443	H25		
C15	VSS_360	VSS_444	H32		
C17	VSS_361	VSS_445	H35		
C19	VSS_362	VSS_446	J10		
C21	VSS_363	VSS_447	J18		
C23	VSS_364	VSS_448	J22		
C25	VSS_365	VSS_449	J25		
C27	VSS_366	VSS_450	J32		
C29	VSS_367	VSS_451	J33		
C31	VSS_368	VSS_452	J36		
C37	VSS_369	VSS_453	J4		
C5	VSS_370	VSS_454	J7		
C8	VSS_371	VSS_455	K1		
C9	VSS_372	VSS_456	K10		
D10	VSS_373	VSS_457	K11		
D12	VSS_374	VSS_458	K2		
D14	VSS_375	VSS_459	K3		
D16	VSS_376	VSS_460	K38		
D18	VSS_377	VSS_461	K4		
D20	VSS_378	VSS_462	K5		
D22	VSS_379	VSS_463	K7		
D24	VSS_380	VSS_464	K8		
D26	VSS_381	VSS_465	K9		
D28	VSS_382	VSS_466	L29		
D3	VSS_383	VSS_467	L30		
D30	VSS_384	VSS_468	L33		
D33	VSS_385	VSS_469	L34		
D6	VSS_386	VSS_470	M12		
D9	VSS_387	VSS_471	M13		
E34	VSS_388	VSS_472	N10		
E35	VSS_389	VSS_473	N11		
E38	VSS_390	VSS_474	N12		
E4	VSS_391	VSS_475	N2		
E9	VSS_392	VSS_476	BT8		
N3	VSS_393	VSS_477	BR9		
N33	VSS_394	VSS_478			
N34	VSS_395	VSS_479			
N4	VSS_396				
N5	VSS_397	VSS_A3	A3		
N6	VSS_398	VSS_A34	A4		
N7	VSS_399	VSS_A4	B3		
N8	VSS_400	VSS_B3	B37		
N9	VSS_401	VSS_B37	BR38		
P12	VSS_402	VSS_BR38	BT3		
P37	VSS_403	VSS_BT3	BT35		
M14	VSS_404	VSS_BT35	BT36		
M6	VSS_405	VSS_BT36	BT4		
N1	VSS_406	VSS_BT4	C2		
F11	VSS_407	VSS_C2	D38		
F13	VSS_408	VSS_D38			

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Title  
CML-H (8/8)

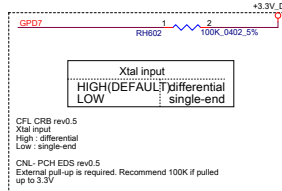
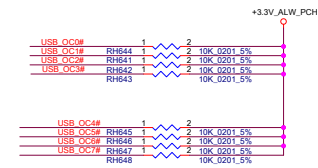
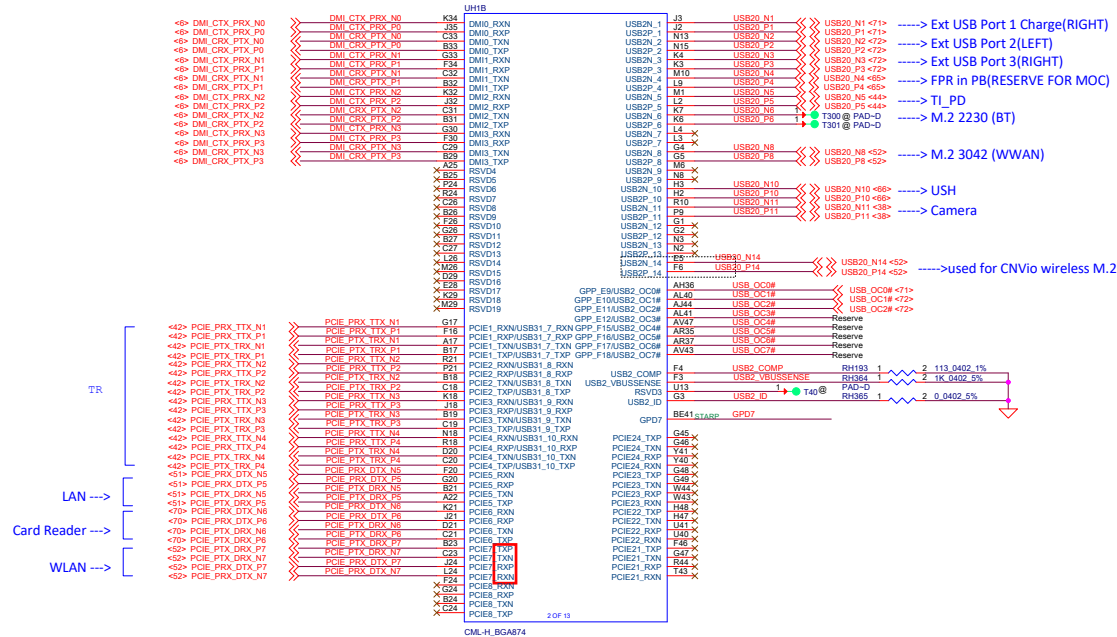
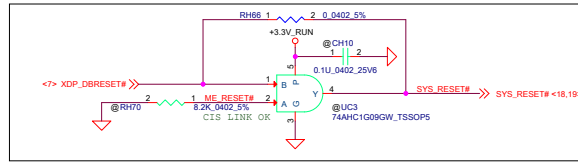
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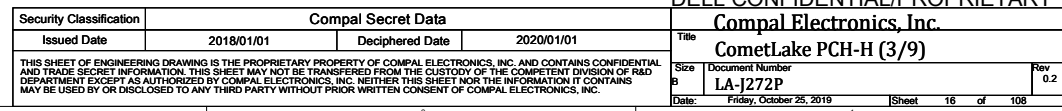
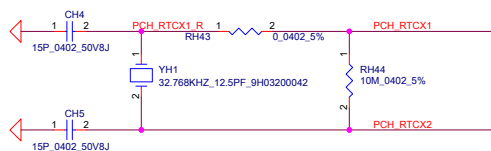
LA-J272P

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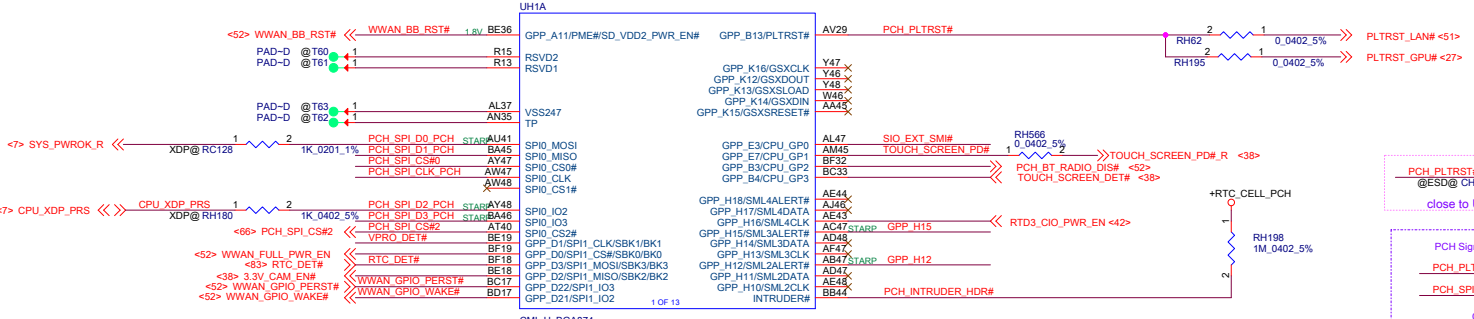
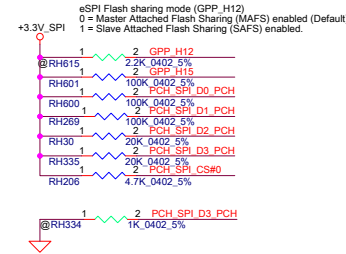
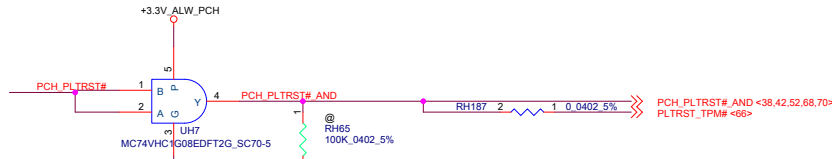
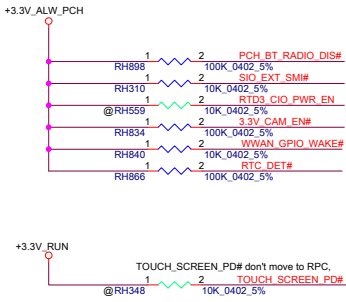
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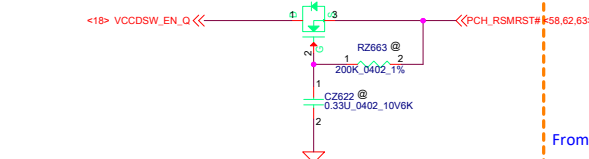




support EC G3 flash

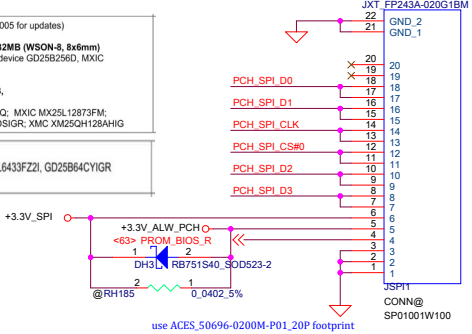
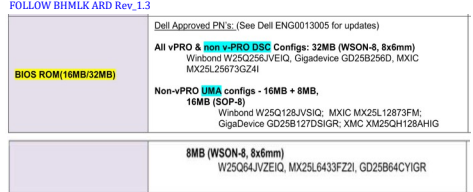
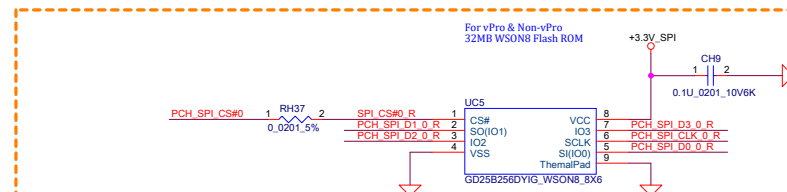
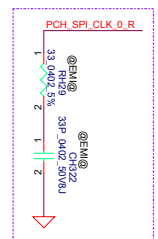
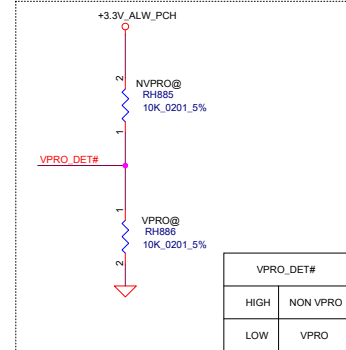
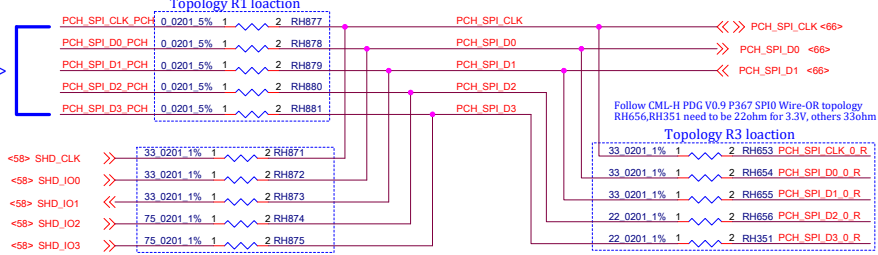


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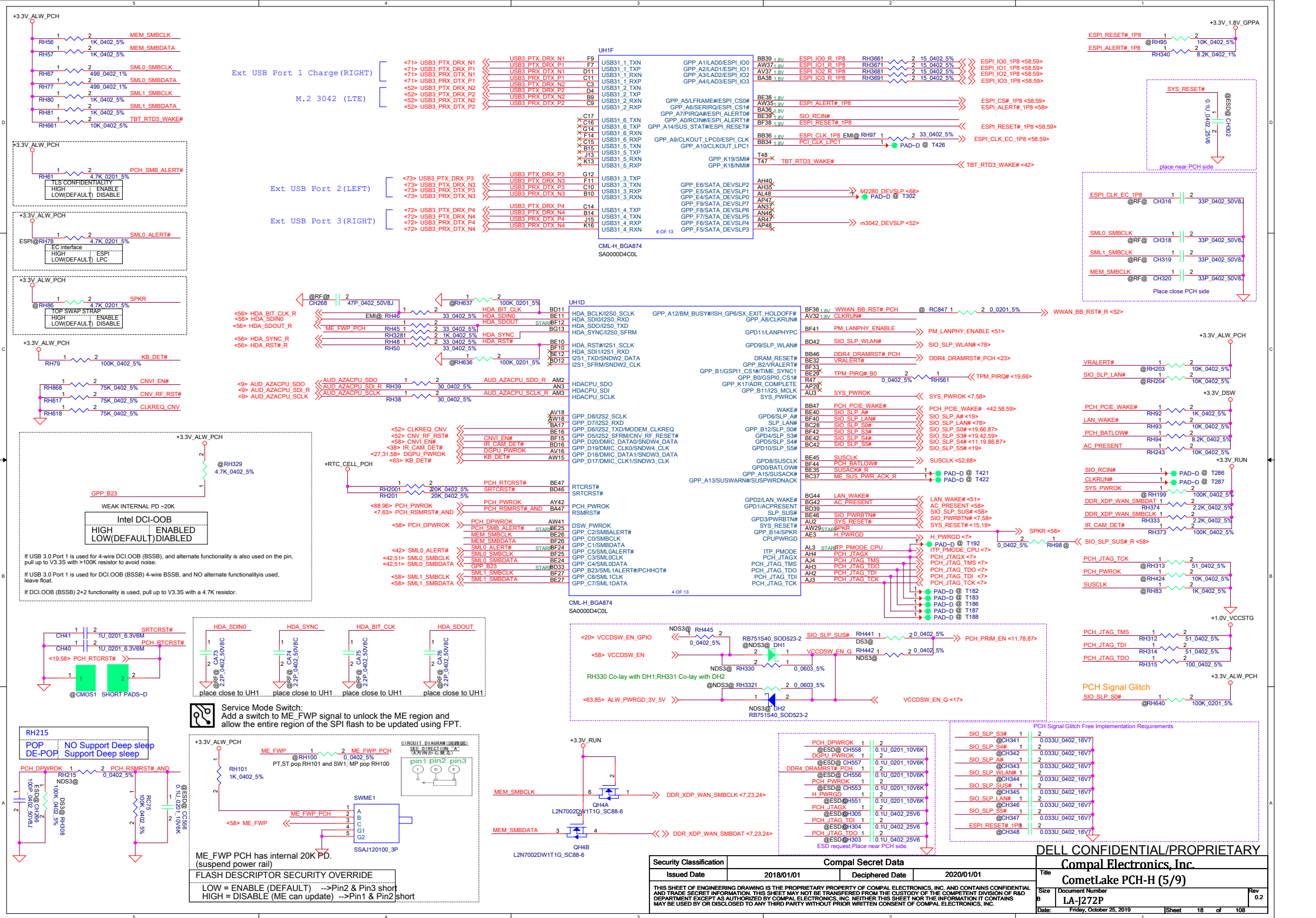


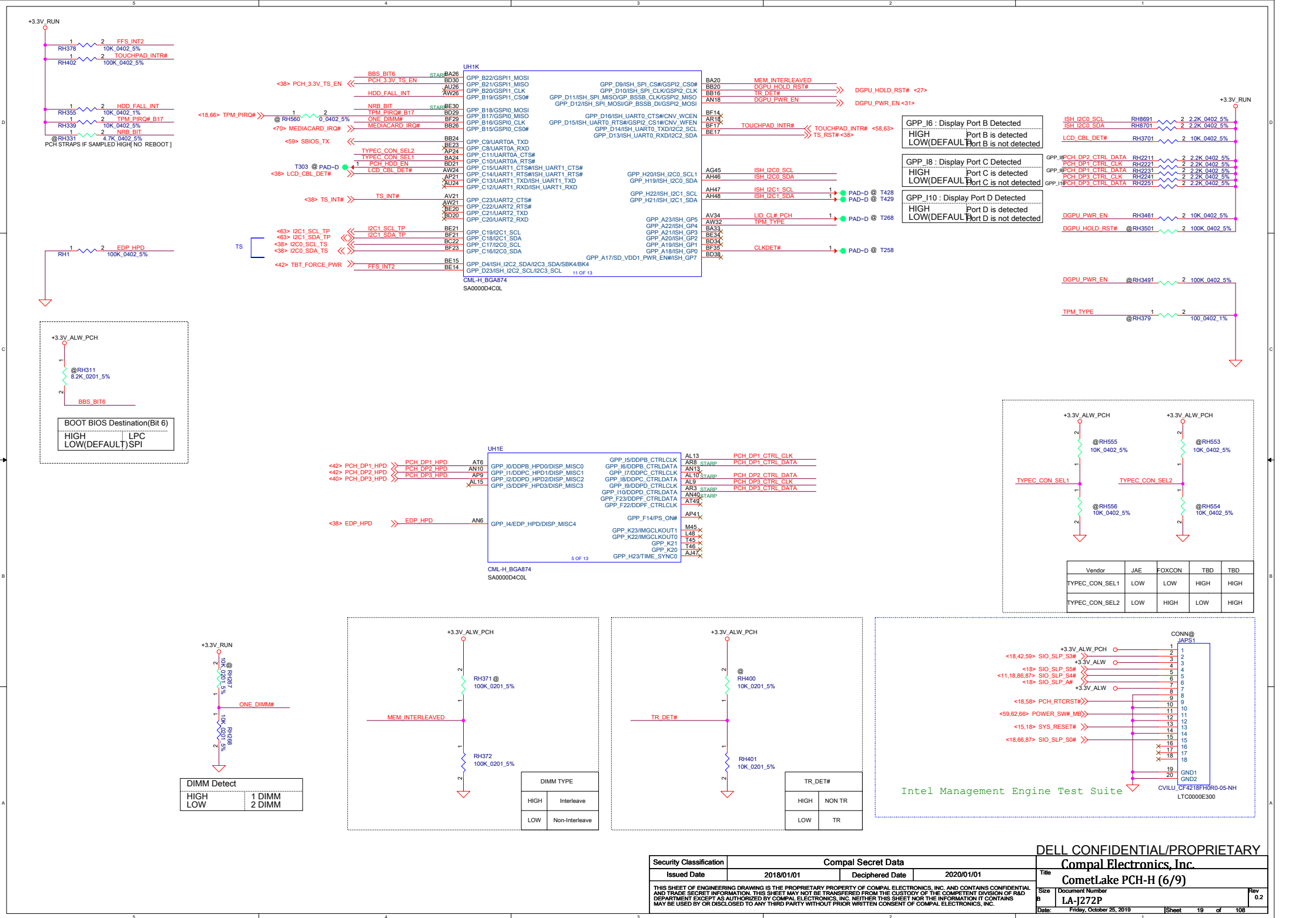
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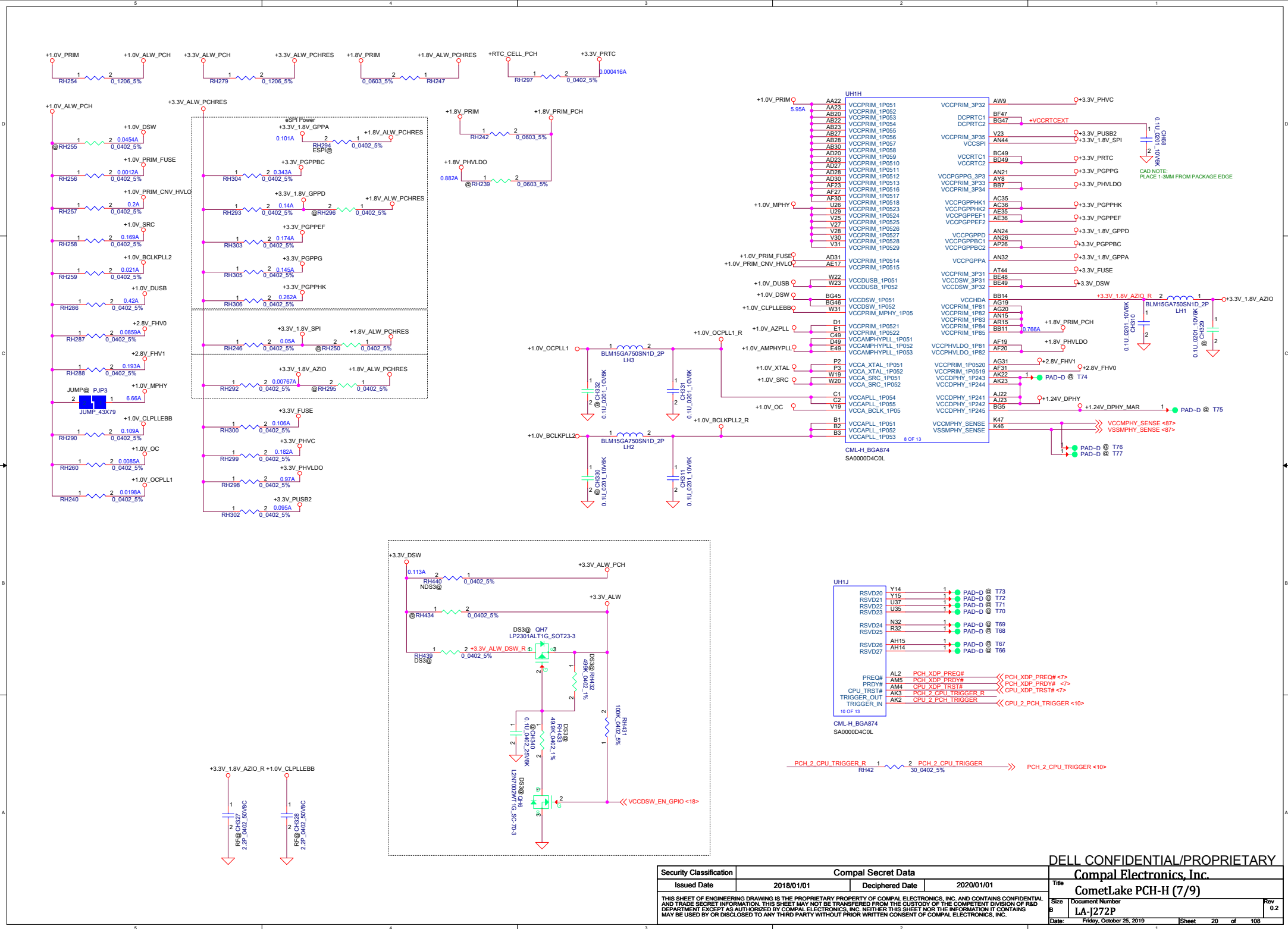
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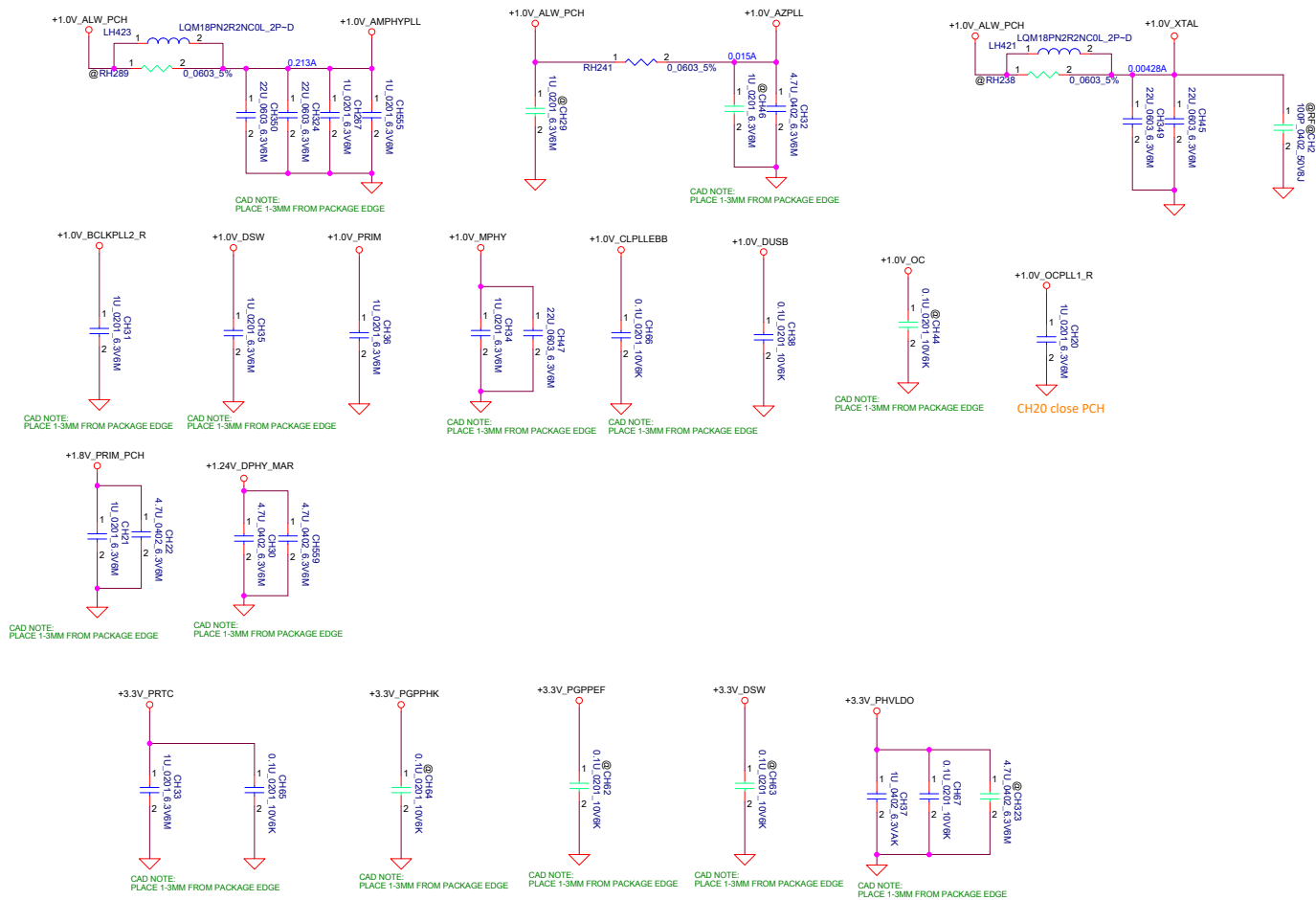


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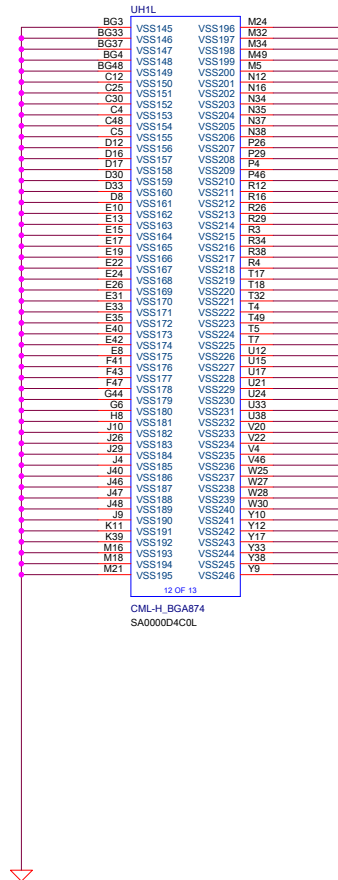


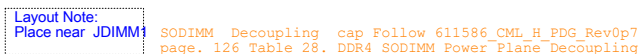




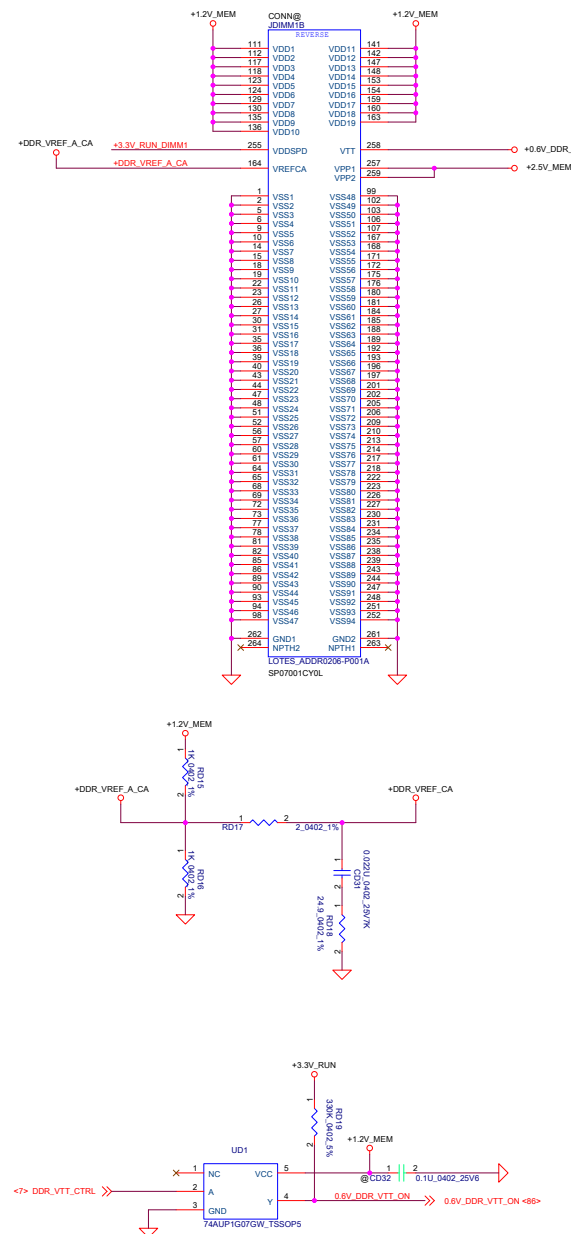
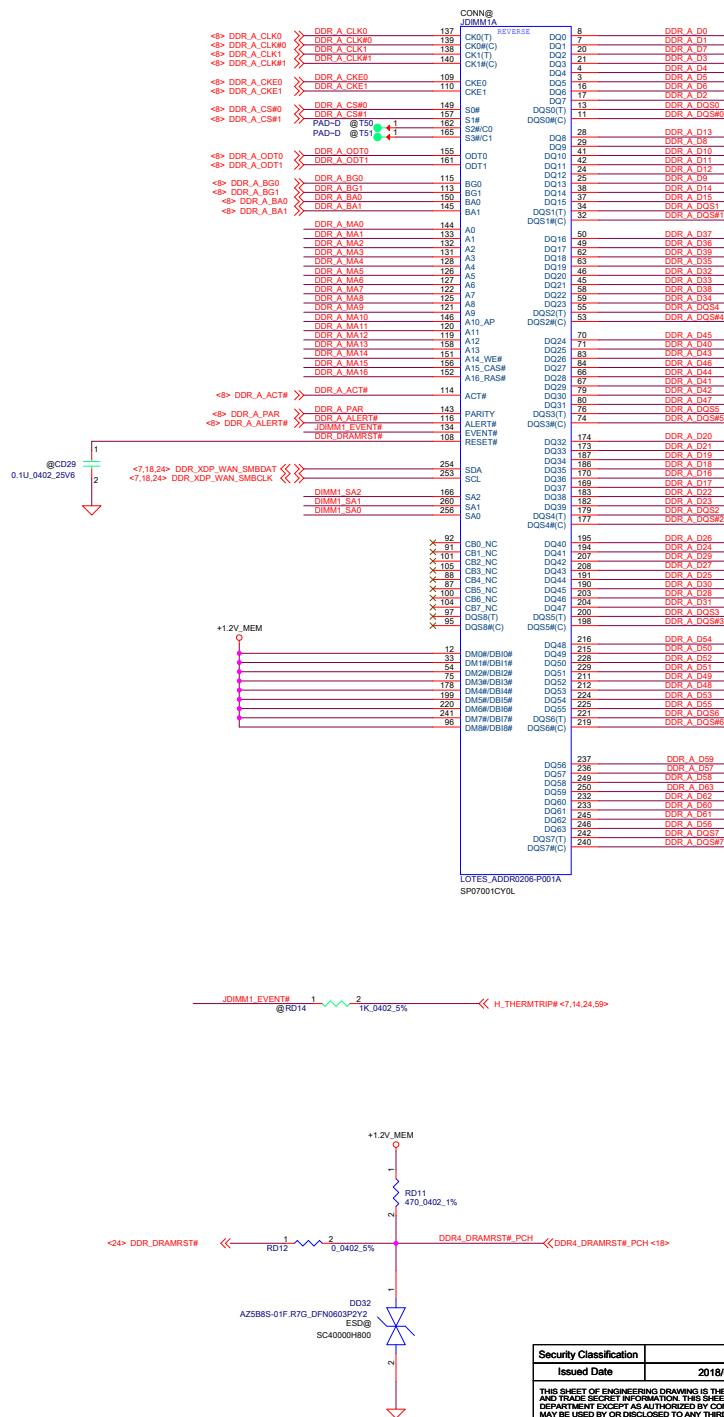
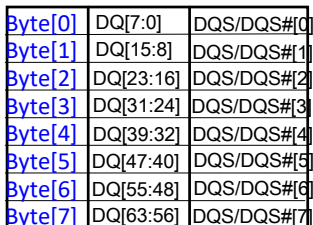


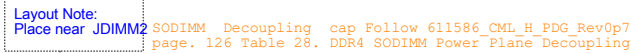
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DIMM3	0	1	0
DIMM4	1	1	0



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Title	<b>DDR4-SODIMM SLOT2</b>

TAL ID	DDR4-SODIMM SE012		
	Size	Document Number	Rev
	C	LA-J272P	0.2
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Size	Document Number		Rev
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Date:	Friday, October 25, 2019	Sheet	25 of 108

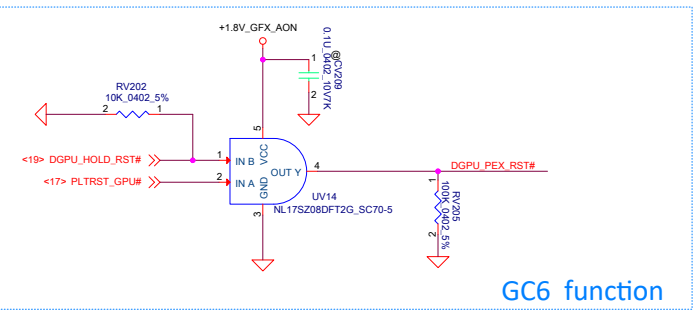
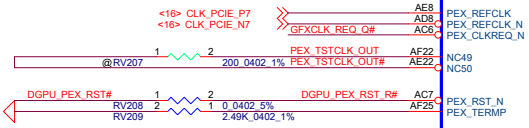
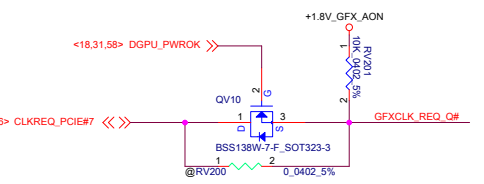
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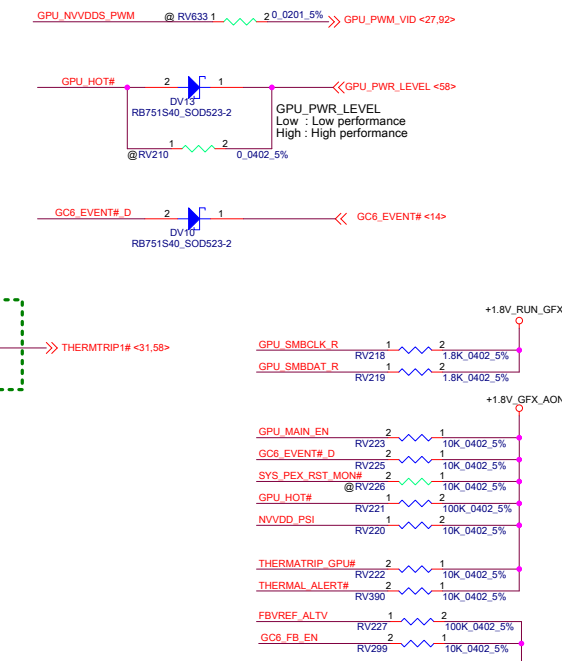
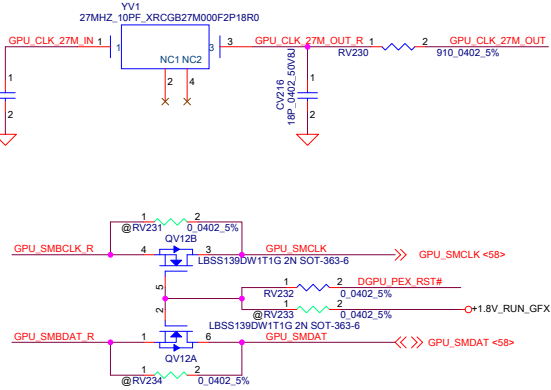
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PEG CRX GTX N9	CV446	2	1	0.22u	0.402	16V7K	PEG CRX C GTX N9
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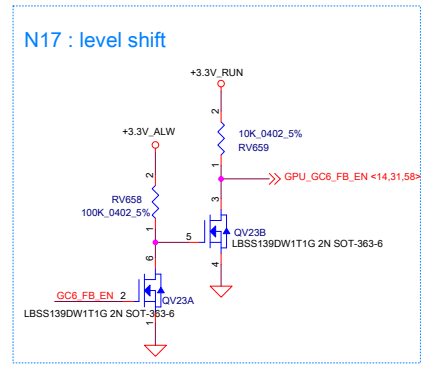
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PEG CTX C GRX P10	AE9	PEG RX2
PEG CTX C GRX N10	AG9	PEG RX2_N
PEG CTX C GRX P11	AG10	PEG RX3
PEG CTX C GRX N11	AG10	PEG RX3_N
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PEG CRX C GTX N11	AB12	PEG TX3_N
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PEG CRX C GTX N8	AC13	PEG TX0_N
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PEG CRX C GTX N9	AC14	PEG TX1_N
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PEG CRX C GTX P11	AC44	PEG TX3
PEG CRX C GTX N11	AC44	PEG TX3_N
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PEG CRX C GTX N8	AC45	PEG TX0_N
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PEG CRX C GTX N9	AC46	PEG TX1_N
PEG CRX C GTX P10	AC47	PEG TX2
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PEG CRX C GTX N11	AC48	PEG TX3_N



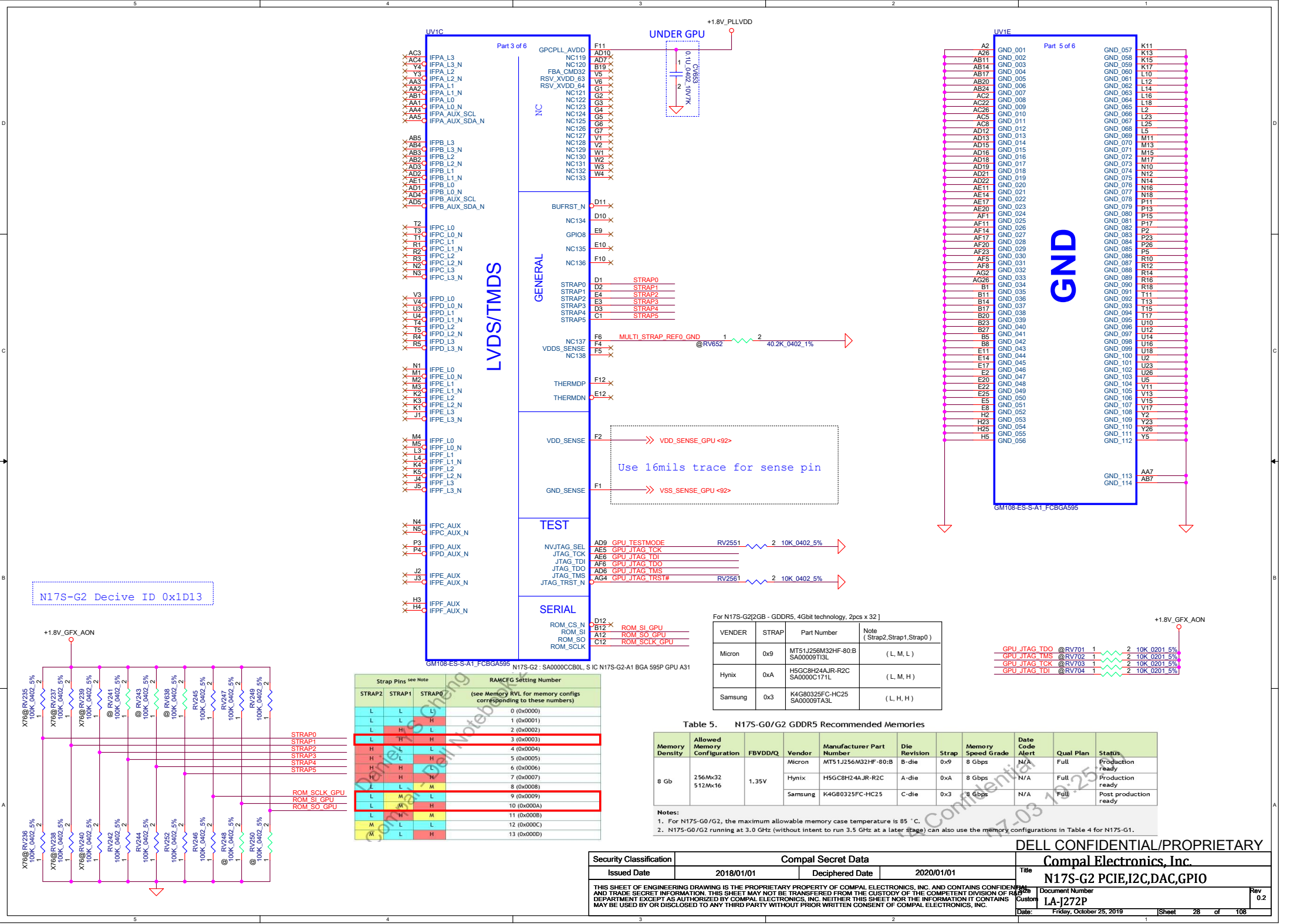
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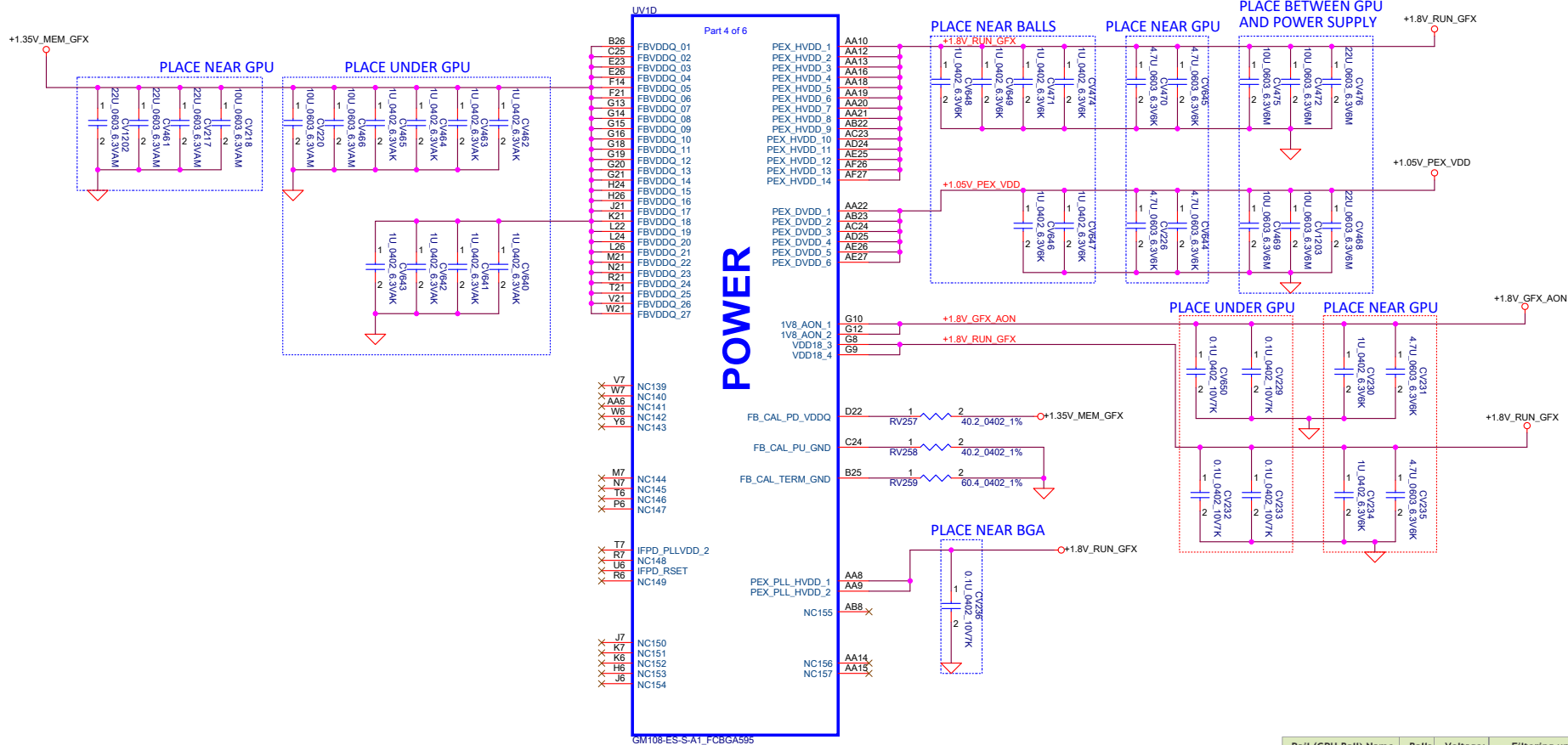


Rail (GPU Ball) Name	Balls	Voltage; Current	Filtering under GPU	Filtering Near GPU
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XS_PLLVDD	1		1 X 0.1uF (0402 X5R)	1 X 22uF (0805)
SP_PLLVDD	1		1 X 0.1uF (0402 X5R)	1 X 4.7uF (0402)
VID_PLLVDD	1		1 X 0.1uF (0402 X5R)	1 X 4.7uF (0402)



N17 : level shift





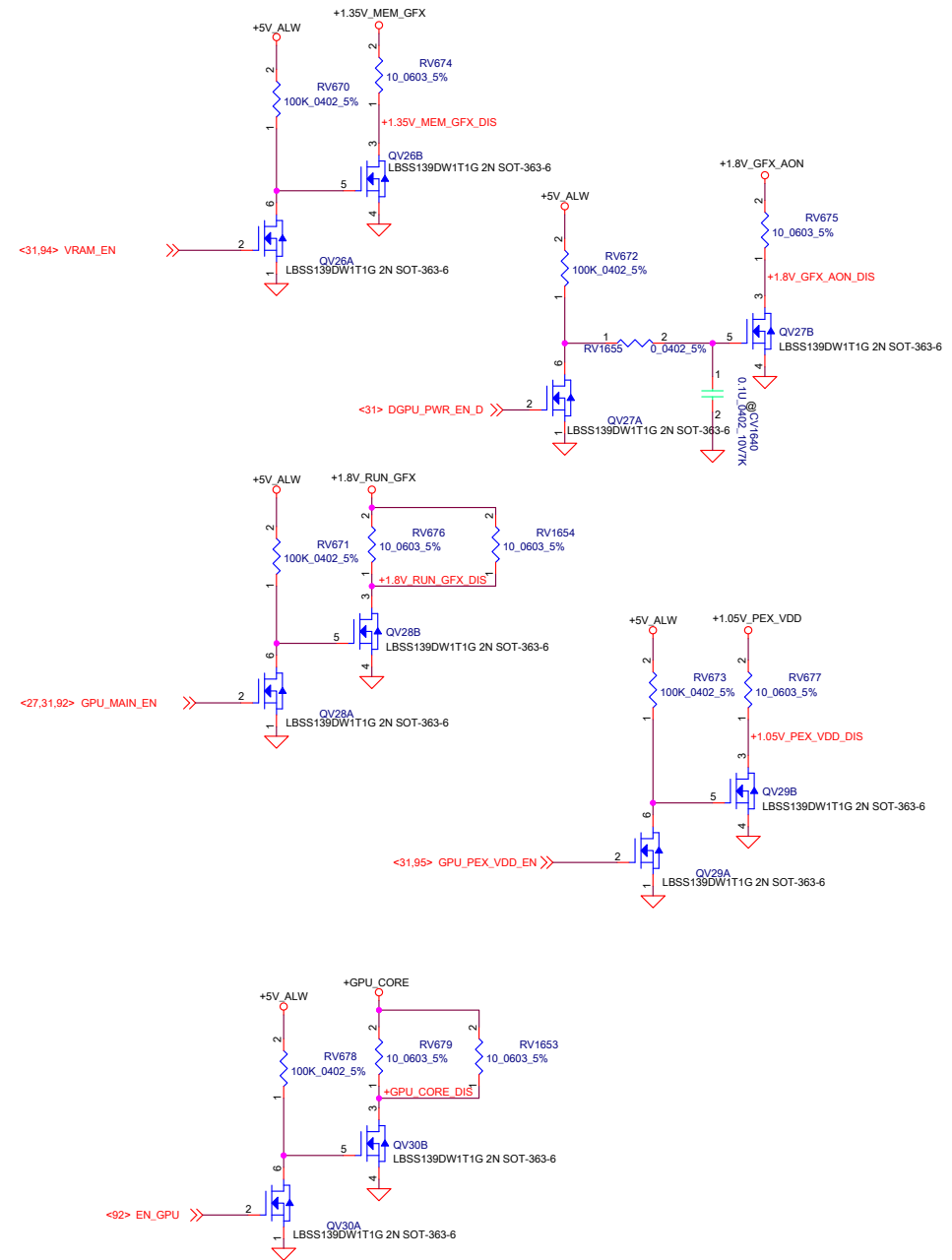
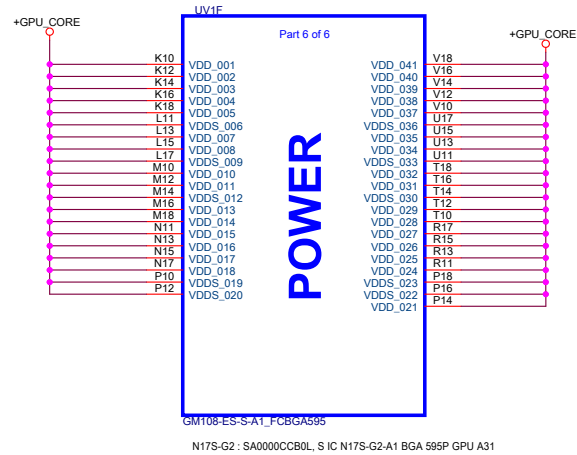
N17S-G2 : SA0000CCB0L, S IC N17S-G2-A1 BGA 595P GPU A31

Rail (GPU Ball) Name	Balls	Voltage; Current	Filtering under GPU	Filtering Near GPU
PEX_DVDD	6	1.0V	2 X 1uF (0402 X5R)	Hear GPU: 2 X 4.7uF (0603) Midway btw GPU & VR: 2 X 10uF (0805) 1 X 22uF (0805)

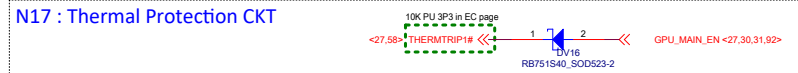
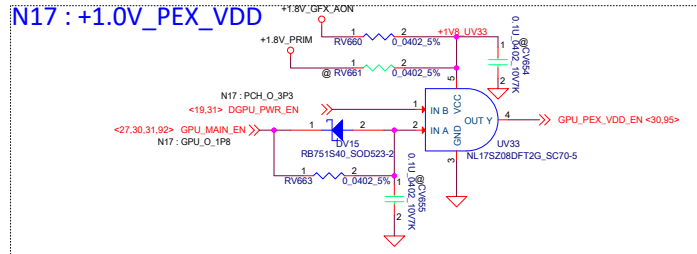
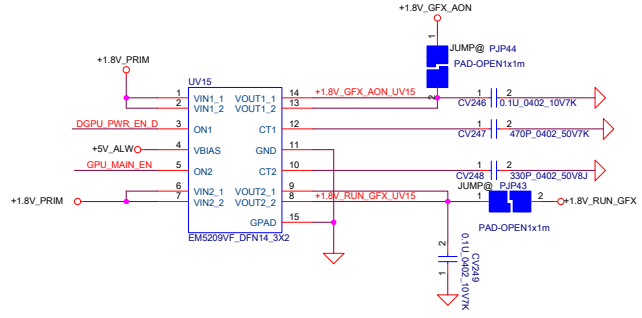
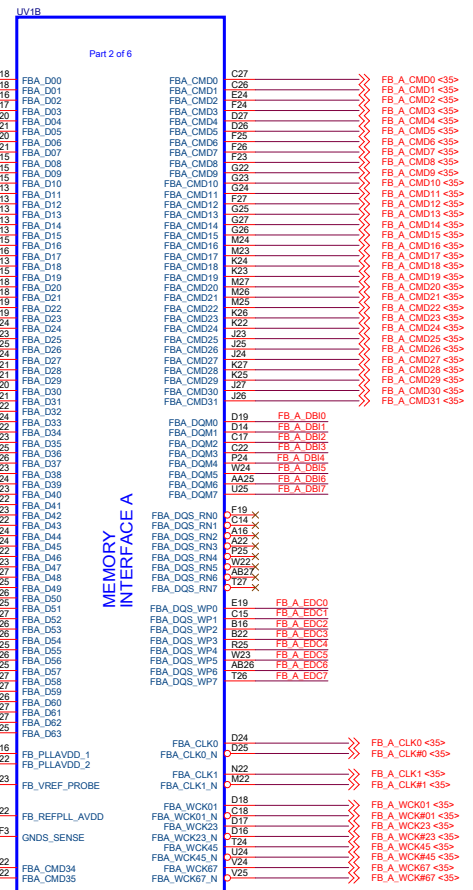
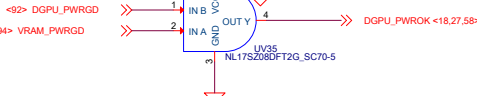
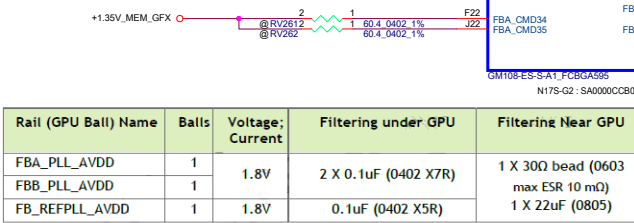
Rail (GPU Ball) Name	Balls	Voltage; Current	Filtering under GPU	Filtering Near GPU
PEX_HVDD	14	1.8V	4 X 1uF (0402 X5R)	Hear GPU: 2 X 4.7uF (0603) Midway btw GPU & VR: 2 X 10uF (0805) 1 X 22uF (0805)
PEX_PLL_HVDD	2	1.8V	1 X 0.1uF (0402)	

Rail (GPU Ball) Name	Balls	Voltage; Current	Filtering under GPU	Filtering Near GPU
FBVDDQ (GPU side) <sup>1</sup>	27	1.35V 1.5V 1.55V	8 X 1uF (0402) 2 X 10uF (0603)	10uF (0603) 3 X 22uF (0603)

Rail (GPU Ball) Name	Balls	Voltage; Current	Filtering under GPU	Filtering Near GPU
1V8_MAIN	2	1.8V	2 X 0.1uF (0402)	1 X 1uF (0402) 1 X 4.7uF (0603)
1V8_AON	2	1.8V	2 X 0.1uF (0402)	1 X 1uF (0402) 1 X 4.7uF (0603)



<0...31>	<32...63>	Memory
CMD0	CMD16	CS#
CMD1	CMD17	A3-BA3
CMD2	CMD18	A2-BA0
CMD3	CMD19	A4-BA2
CMD4	CMD20	A5-BA1
CMD5	CMD21	WE#
CMD6	CMD22	A6-A8
CMD7	CMD23	A6-A11
CMD8	CMD24	AB#
CMD9	CMD25	A0-A7 FRU
CMD10		A0-A10
CMD11	CMD27	A1-A9
CMD12	CMD28	RAS#
CMD13	CMD29	CKE#
CMD14	CMD30	CKE#
CMD15	CMD31	CAS#

[illegible]

# Reserve

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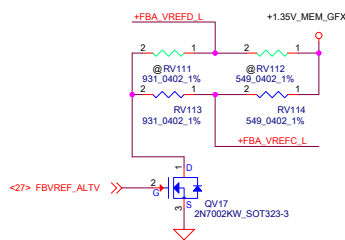
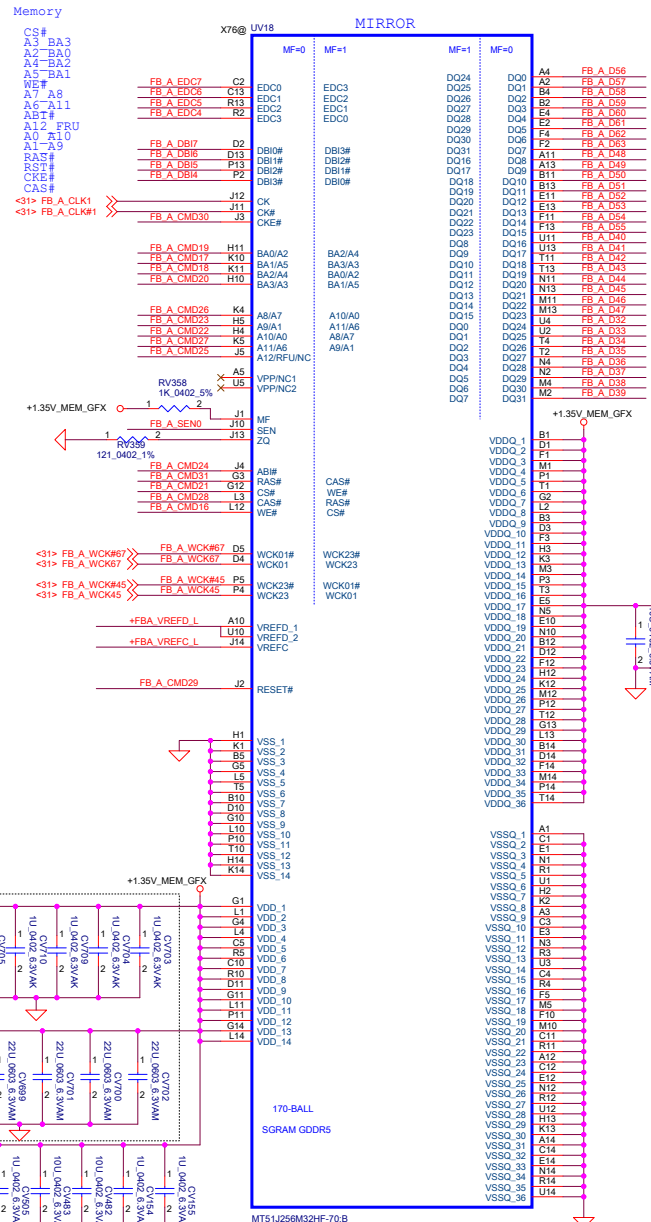
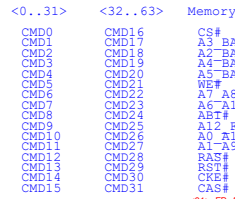
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```
<31> FB_A_D[0..63] << >> FB_A_D[0..63]
<31> FB_A_EDC[0..7] << >> FB_A_EDC[0..7]
<31> FB_A_DB[0..7] << >> FB_A_DB[0..7]
<31> FB_A_CMD[0..31] << >> FB_A_CMD[0..31]
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				Document Number			
				LA-1727P			
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DGPU_DC/DC Interface			
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CRT		
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## Reference Titan Ridge SP 1.41 Datasheet

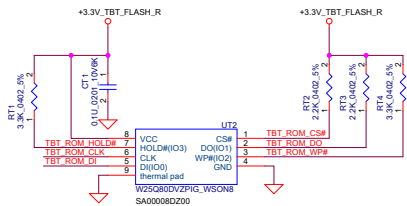
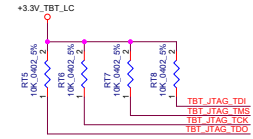
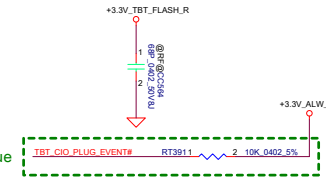


Table 12. Supported types of Flash Memory

Manufacturer	Type	Volume, Mbit	Supply, V
Giga Device	GD25Q80C	8.0	2.7-3.6
Giga Device	GD25Q80CTIG	8.0	3.3
EON	EN25Q80B	8.0	2.7-3.6
FMSH	FM25Q08	8.0	2.7-3.6
Macronix	MX25L8006EM1I	8.0 (150mil, 8-SOP)	2.7-3.6
Winbond	W25Q80DL	8.0	2.3-3.6



For backdrive issue



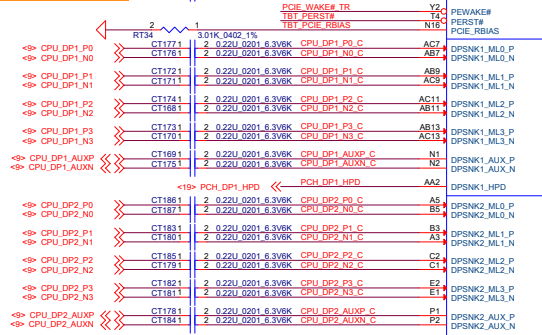
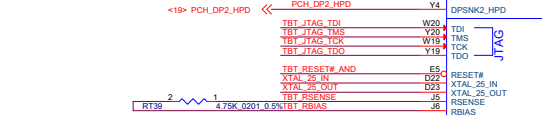
connect to PCH



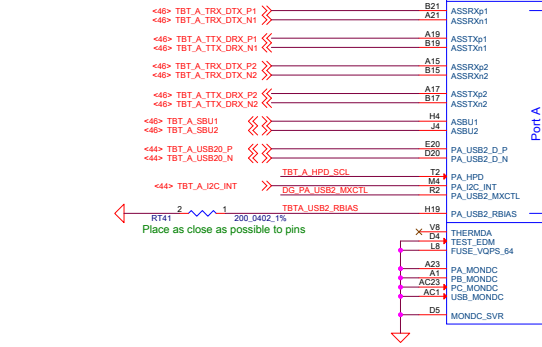
connect to PCH



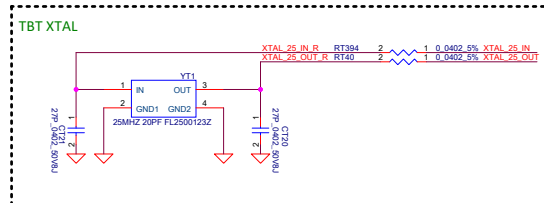
CF  
DF

CPU  
DDI2

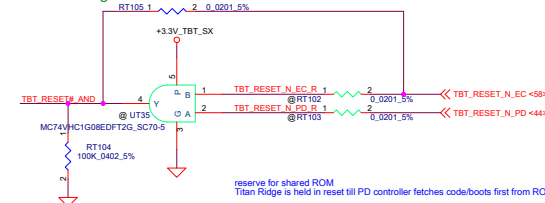
ype-C



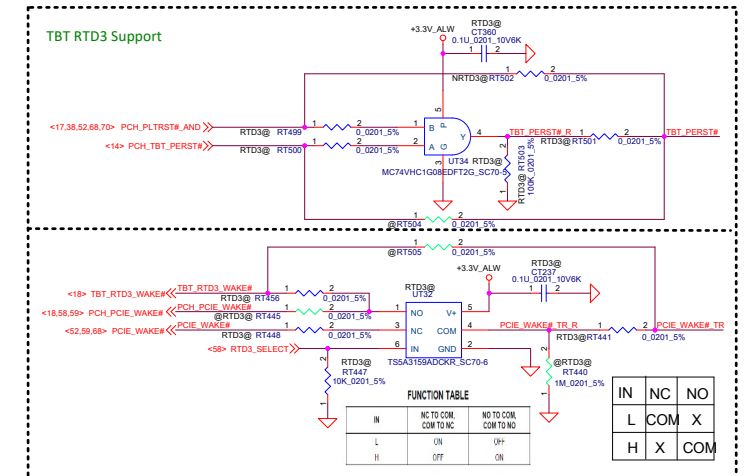
Place as close as possible to pins



### TBT Reset AND gate



reserve for shared ROM  
Titan Ridge is held in reset till PD controller fetches code/boots first from RC



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TBT-TR-SP(1/2)

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Custom	LA 1272D	0.2

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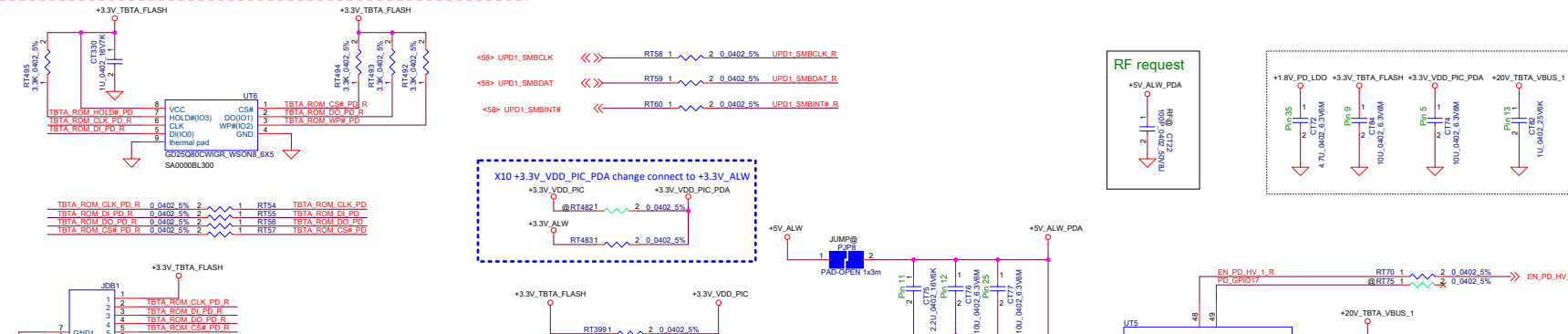
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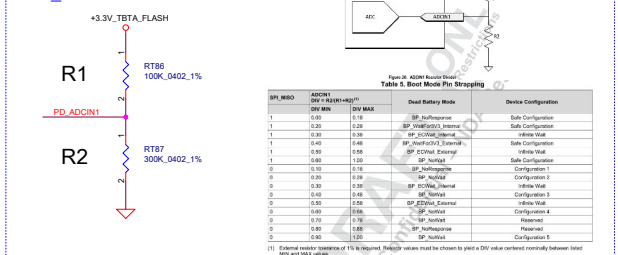
**FOLLOW X11 NB MLK(0508) PD 65982DD change to 65987DD**



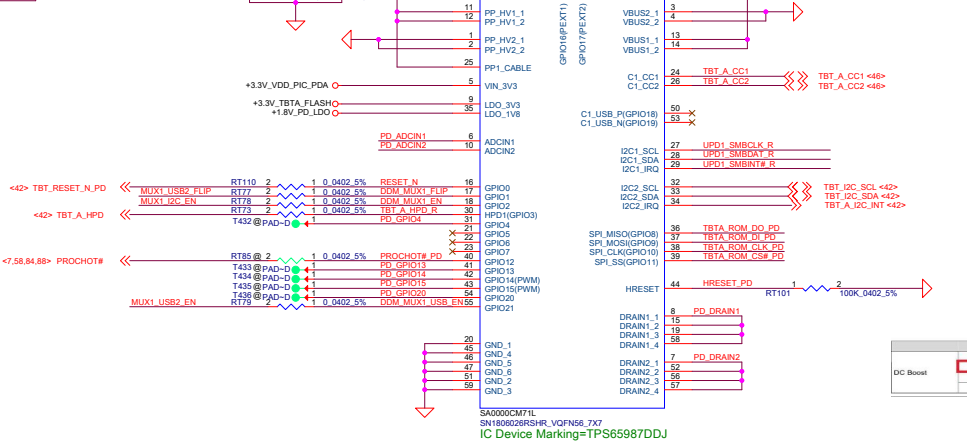
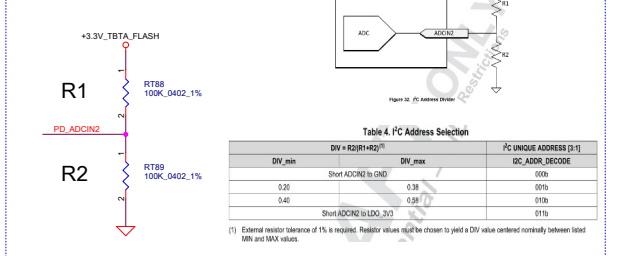
**PD GPIO define**

GPIO	Pin #	Package Pin Name	TP56988B (Dual Port)	TP56987S (Single Port)	NOTES
0	16	GPIO0 (RESET)	TR_RESET	TR_RESET	
1	17	GPIO1	DDM_MUX1_FLIP	DDM_MUX1_FLIP	GPIO for I2C/USB2.0 Mux control
2	18	GPIO2	DDM_MUX2_EN	DDM_MUX2_EN	
3	30	GPIO3 (HPD1)	TR_PA_HPD	TR_PA_HPD	HPD/SMBUS_vho
4	31	GPIO4 (HPD2)	TR_PA_HPD	TR_PA_HPD	
5	21	GPIO5	-	-	Rev1 I2C/SPI for external DP-USB3 Mux control
6	22	GPIO6	-	-	
7	23	GPIO7	-	-	
8	36	SPI_MISO (Boot Mode)	SPI_MISO	SPI_MISO	Backup SPI Flash
9	37	SPI_MOSI (GPIO3)	SPI_MOSI	SPI_MOSI	
10	38	SPI_CLK (GPIO10)	SPI_CLK	SPI_CLK	
11	39	SPI_SS (GPIO11)	SPI_SS	SPI_SS	
12	40	GPIO12 (SWD)	PROCHOT#	PROCHOT#	PD config as OD for shared use Rev1 for DDM_MUX2_USB_EN
13	41	GPIO13 (SWD)	-	-	
14	42	GPIO14 (SWD)	DDM_MUX1_FLIP	DDM_MUX1_FLIP	GPIO for I2C/USB2.0 Mux control
15	43	GPIO15 (SWD)	DDM_MUX2_EN	DDM_MUX2_EN	
16	48	GPIO16 (PP_EXT1)	PP3_HV1_EN	PP3_HV1_EN	
17	49	GPIO17 (PP_EXT2)	PP4_HV1_EN	PP4_HV1_EN	
18	50	GPIO18 (CL_USB_P)	-	-	Rev1 I2C/SPI for external DP-USB3 Mux control
19	51	GPIO19 (CL_USB_N)	-	-	
20	54	GPIO20 (C2_USB_P)	-	-	Rev1 for DDM_MUX2_USB_EN
21	55	GPIO21 (C2_USB_N)	-	-	
22	24	CL_C1	Port1 CC	Port1 CC	Port1 CC
23	25	CL_C2	Port2 CC	Port2 CC	Port2 CC
24	47	C2_C2	Port2 CC	Port2 CC	Port2 CC
25	6	ADIN0L	Buspower Config	Buspower Config	
26	10	ADIN0H (I2C_Add)	Pull Dn (0x20, 0x24)	Pull Dn (0x20, 0x24)	I2C Address config
27	27	I2C1_SCL (Master/Slave)	I2C1 for EC	I2C1 for EC	
28	28	I2C1_SDA (MPS)	I2C1 for EC	I2C1 for EC	
29	29	I2C1_IRQ (MPS)	-	-	
30	32	I2C2_SCL (Slave Only)	I2C2 for TR	I2C2 for TR	
31	33	I2C2_SDA (Slave)	I2C2 for TR	I2C2 for TR	
32	34	I2C2_IRQ (Slave)	I2C2 for TR	I2C2 for TR	

**BUSPOWER Config BP\_NoWait value 0.7~0.78**



**Need CHECK I2C Address Divider:010b**

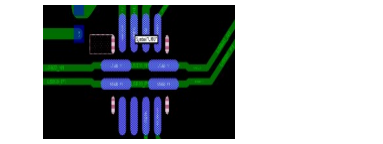
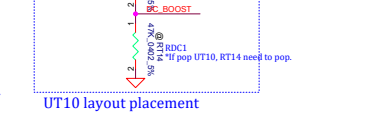


PARAMETER	VALUE
VCC (0.9V to 3.3V)	3.3 V
AC Boost	No

PARAMETER	VALUE
DC Boost	22 mV ~ 47 mV
DC Boost	22 mV ~ 47 mV

PARAMETER	VALUE
DC Boost	22 mV ~ 47 mV
DC Boost	22 mV ~ 47 mV

**DC BOOST**



ENA	ENB	INA	INB	OUTA1	OUTA2	OUTB1	OUTB2
0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0
1	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0

BA1	BA2	BA3	BA4	BA5	BA6	BA7	BA8
0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0
1	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0

BA1	BA2	BA3	BA4	BA5	BA6	BA7	BA8
0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0
1	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0

BA1	BA2	BA3	BA4	BA5	BA6	BA7	BA8
0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0
1	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0

BA1	BA2	BA3	BA4	BA5	BA6	BA7	BA8
0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0
1	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0

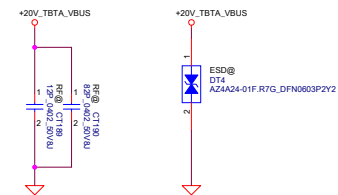
BA1	BA2	BA3	BA4	BA5	BA6	BA7	BA8
0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0
1	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0

BA1	BA2	BA3	BA4	BA5	BA6	BA7	BA8
0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0
1	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0

BA1	BA2	BA3	BA4	BA5	BA6	BA7	BA8
0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0
1	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0

Reserve

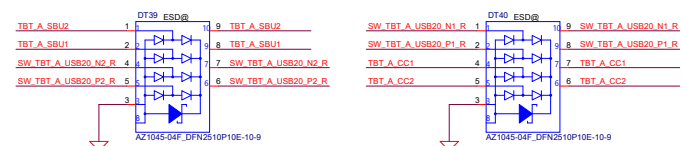
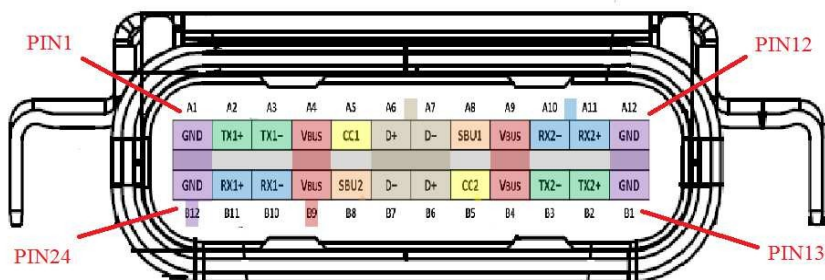
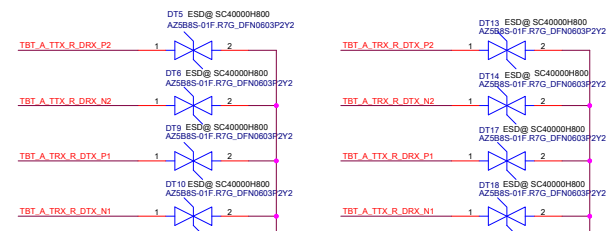
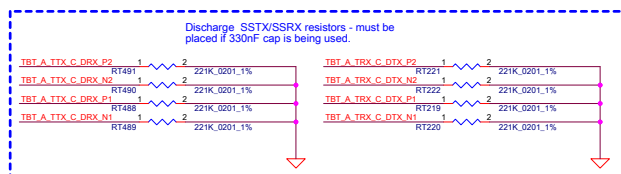
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Place holder for future VBUS-short fix (reduce current usage)

AC coupling is recommended for VBUS-short protection on STSX/SXRX lines. If not needed, place 0 Ohm resistor instead.

Signal	Pin	Resistor
TBT_A.TRX.DTX.P1	RT190	2.2 0.001 Ω
TBT_A.TRX.DTX.N1	RT191	2.2 0.001 Ω
TBT_A.TTX.DRX.P1	RT192	2.2 0.001 Ω
TBT_A.TTX.DRX.N1	RT193	2.2 0.001 Ω
TBT_A.TRX.DTX.P2	RT194	2.2 0.001 Ω
TBT_A.TRX.DTX.N2	RT195	2.2 0.001 Ω
TBT_A.TTX.DRX.P2	RT196	2.2 0.001 Ω
TBT_A.TTX.DRX.N2	RT197	2.2 0.001 Ω



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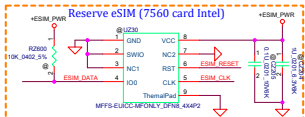
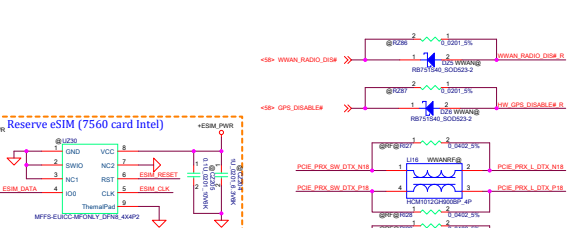
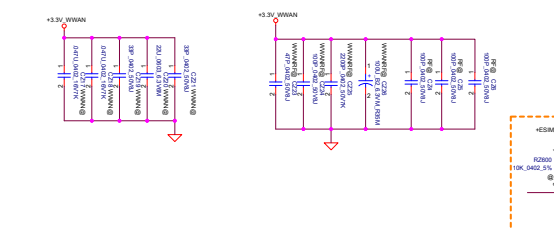
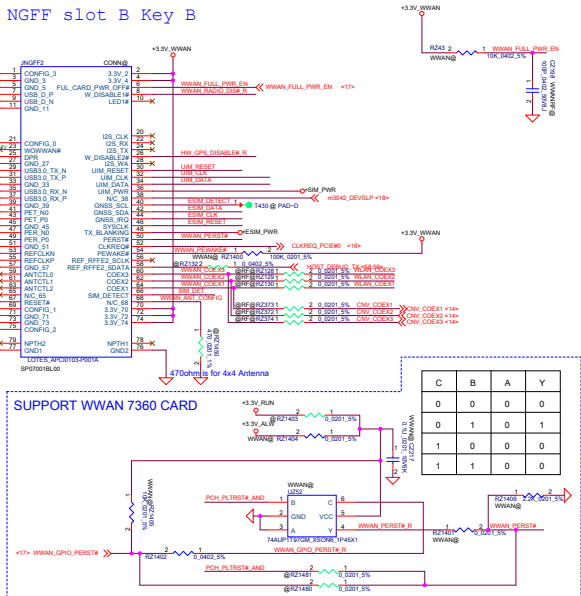
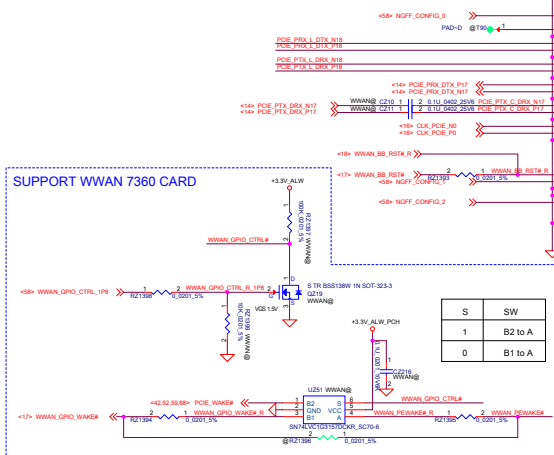


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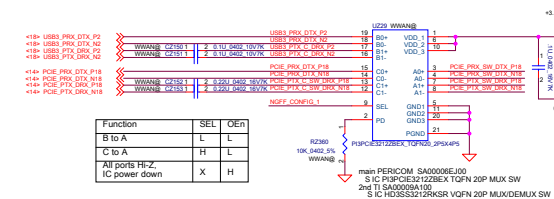
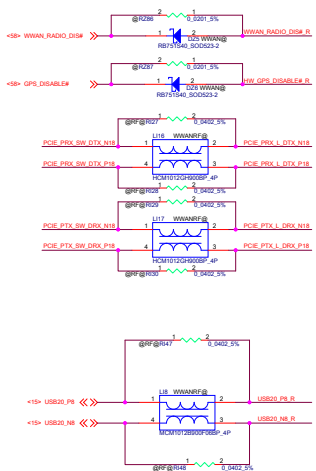
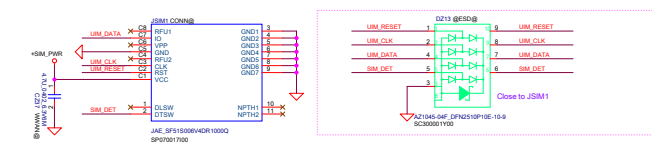
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Reserve TYPE-C Power Path		
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NGFF slot B Key B



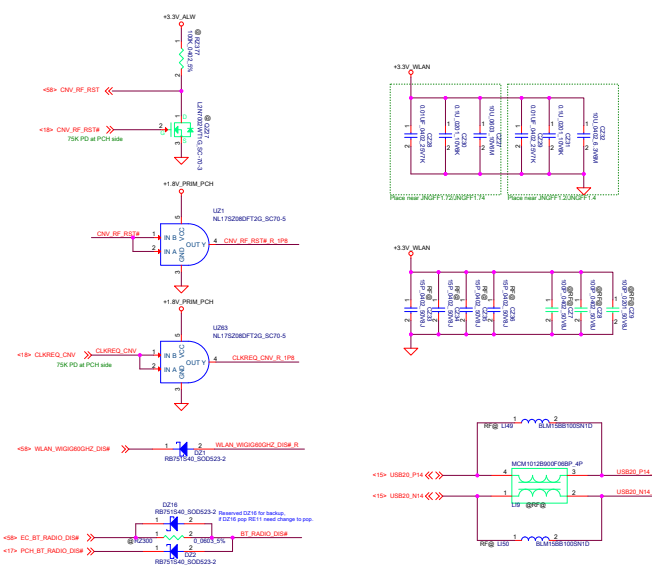
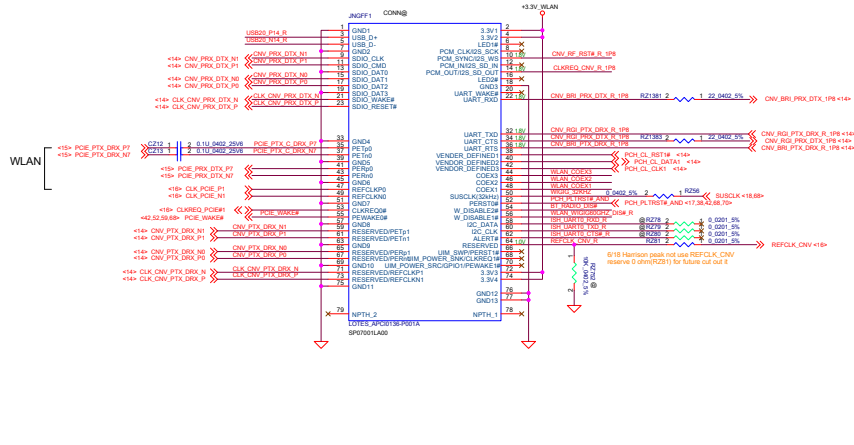
## SIM Card Push-Push



Function	SEL	OEn
B to A	L	L
C to A	H	L
All ports Hi-Z, IC power down	X	H

EJ00  
TQFN 20P MUX SW  
VQFN 20P MUX/DEMUX SW

## NGFF slot E Key E



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ISSUED DATE	2015/01/01	Deciphered Date	2020/01/01
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Size	Document Number			Rev
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Size	Document Number				Rev
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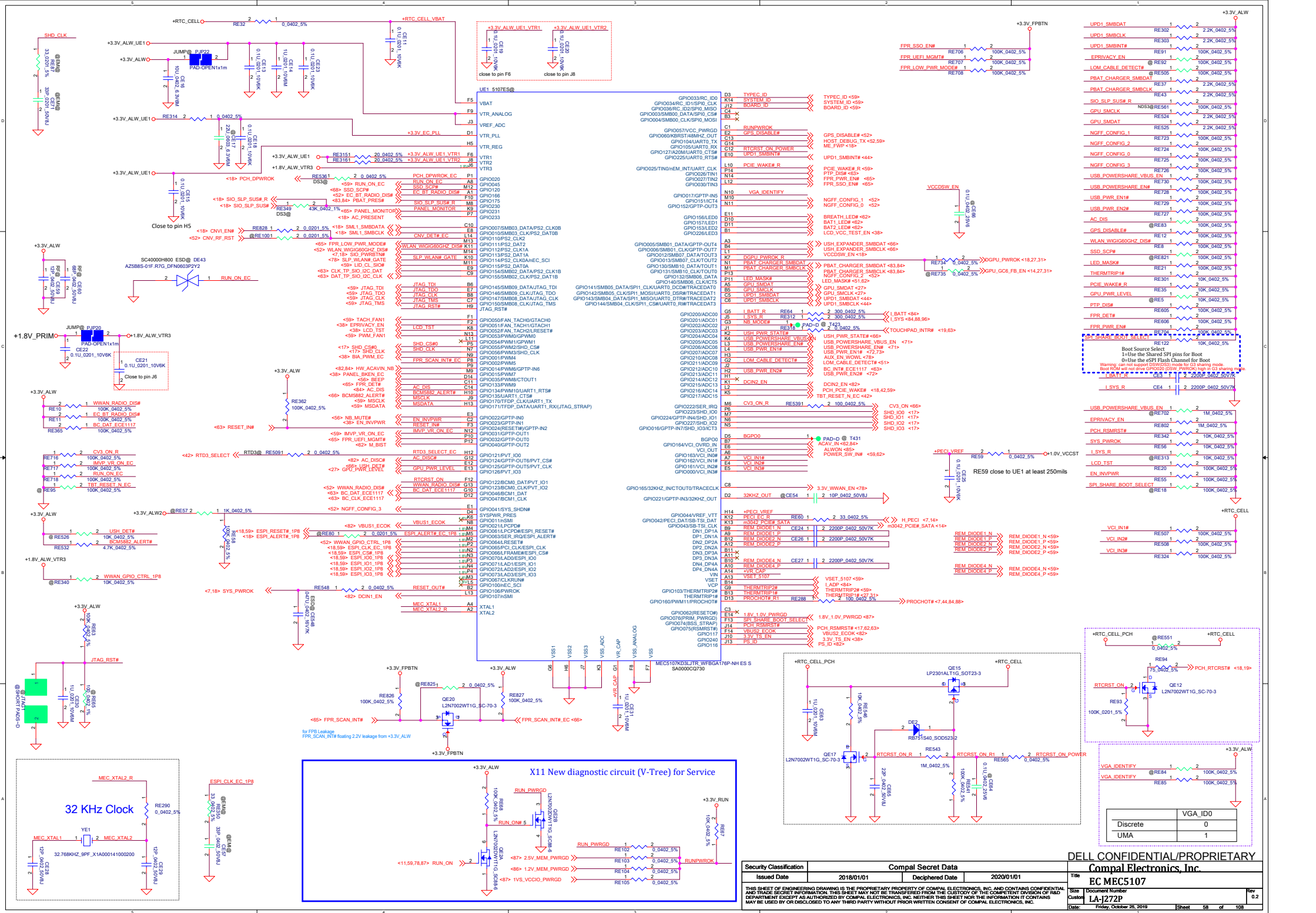
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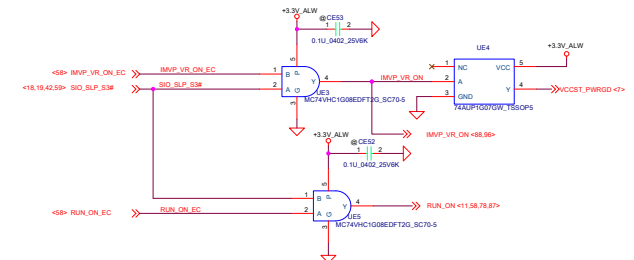
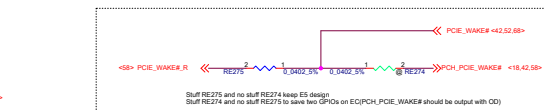
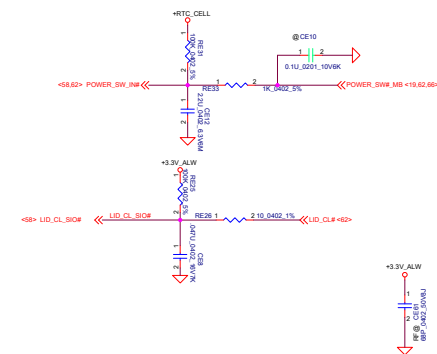
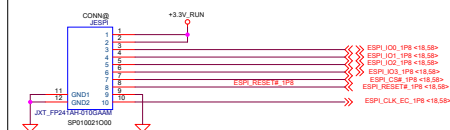


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Title		
Audio Ampfilter		
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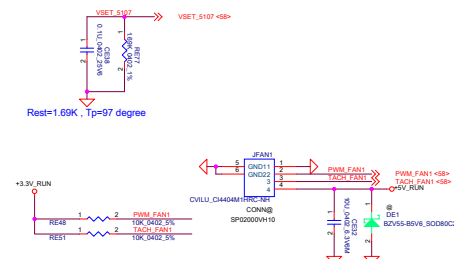
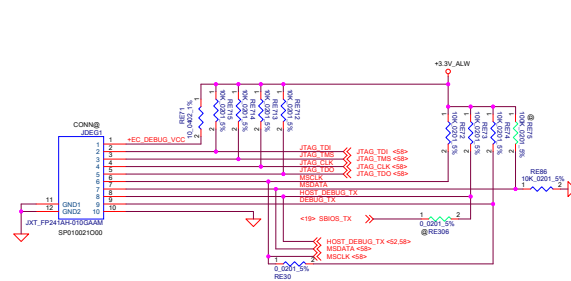


RE343	CE62	REV
240K	4700p	Single Port ACE w/o TR
130K	4700p	Single Port ACE w/ TR
62K	4700p	Dual Port ACE w/o TR
33K	4700p	Dual Port ACE w/ TR
8.2K	4700p	Dual Port ACE (w/ TR + w/o TR)
4.3K	4700p	
2K	4700p	
1K	4700p	

RE79	CE40	REV
240K	4700p	X00
130K	4700p	X01
62K	4700p	X02
33K	4700p	X03
8.2K	4700p	
4.3K	4700p	A00
2K	4700p	
1K	4700p	

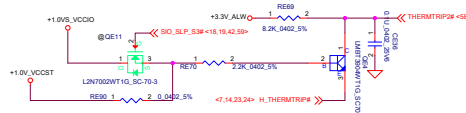
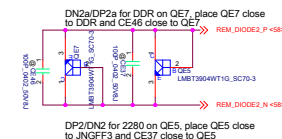
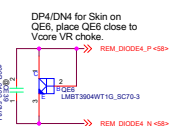
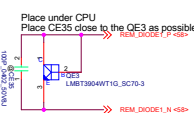
RE300	CE47	PANEL SIZE
240K	4700p	11"
130K	4700p	12"
62K	4700p	13"
33K	4700p	14"
8.2K	4700p	BR15 H
4.3K	4700p	17"
2K	4700p	BR15 P
1K	4700p	

PD ACE DET# rise time is measured from 5% - 48% BOARD ID rise time is measured from 5% - 48% PANEL ID rise time is measured from 5% - 48%.



#### Thermal diode mapping

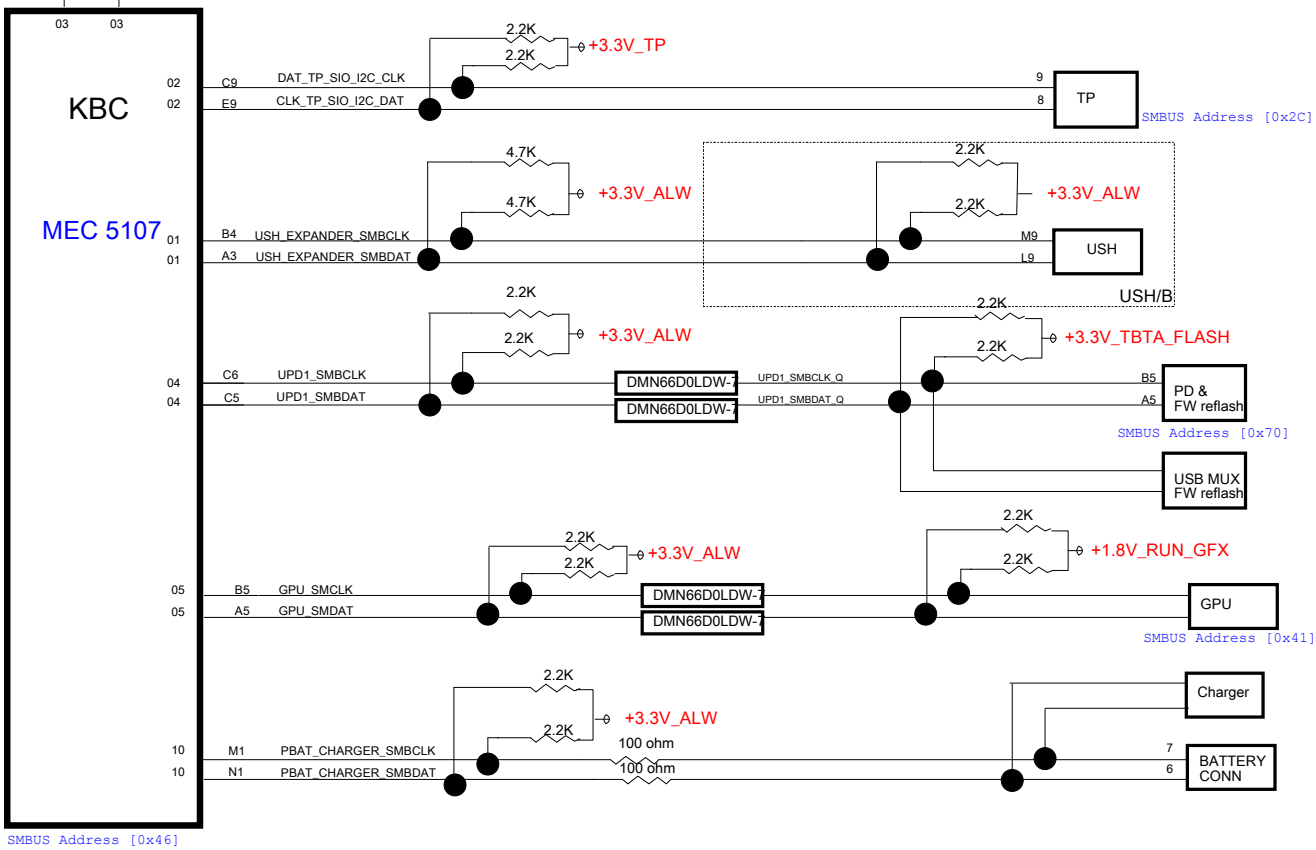
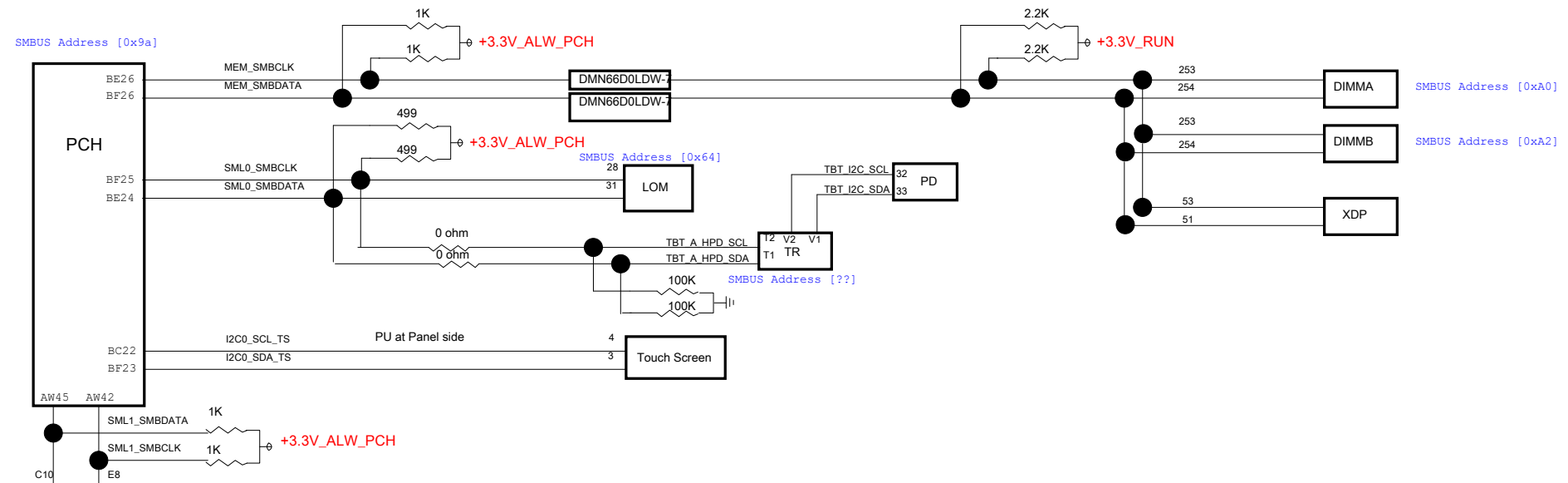
5107 Channel	Location
DP1/DN1	CPU (QE3)
DP2/DN2	2280 (QE5)
DN2a/DP2a	DDR (QE7)
DP3/DN3	NA
DP4/DN4	CPU VR (QE6)



# Reserve

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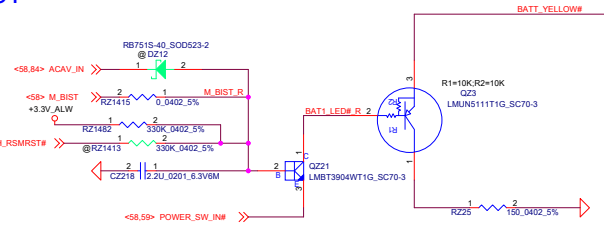
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Title			
Secure & Reset IC			
Size	Document Number		Rev
	LA-J272P		0.2
Date:	Friday, October 25, 2019		Sheet 60 of 108



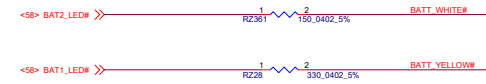
DEVICE	SLAVE ADDRESS	COMMENT
MEMORY	DIMM1=0xA0 DIMM2=0xA2	FFS=0101001b
LAN	I219LM:0x64 I219V:0x64	
EC	0x98	
Touch screen	0x10 & 0x4A	
PD2	Reserved	
USH	0xA4	
Touch pad	0x2C	
PD1	0x44	
GPU	TBD	

X10 14 inch Touch Screen I2C Address				
VENDOR	AUO	LGD	INX	
VPN	AF06	E430	AE0D	
Touch Controller	Elan	Melfas	Elan	
slave address	0x10	0x34	0x10	
HID address	Yes	Yes	Yes	
7-bit address	0x0001	0x0000	0x0001	

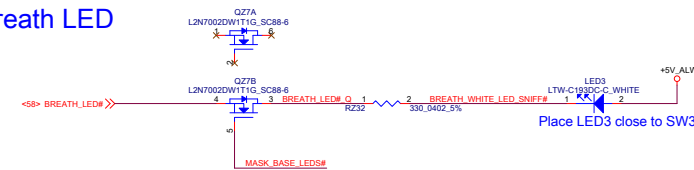
## M BIST



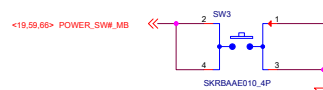
## Battery LED



## Breath LED

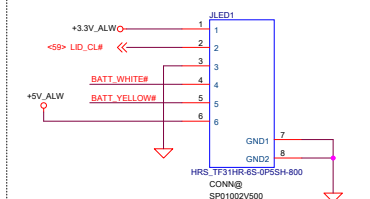


## POWER & INSTANT ON SWITCH

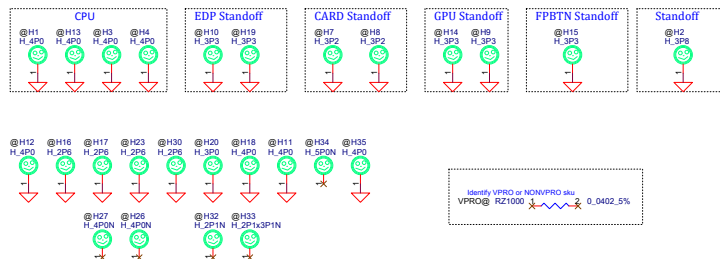
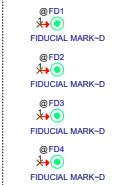


LED Circuit Control Table		
	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Unobtrusive mode)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1

## LED board CONN



### Fiducial Mark



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## Touch Pad

The schematic diagram illustrates the Touch Pad I2C interface. It features two I2C controllers: "I2C From EC" and "I2C From CPU".

**I2C From EC:**

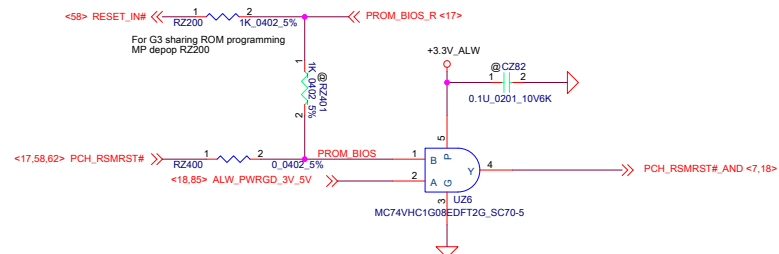
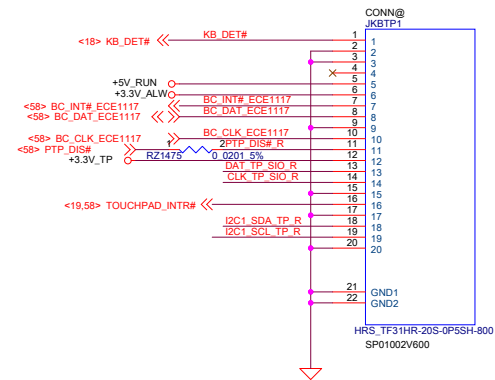
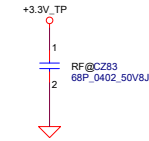
- The **DAT\_TP\_SIO\_I2C\_CLK** pin is connected to the **@RZ22** pin (0.0402 5% resistor).
- The **CLK\_TP\_SIO\_I2C\_DAT** pin is connected to the **@RZ23** pin (0.0402 5% resistor).
- The **I2C1\_SDA\_TP\_R** pin is connected to the **RZ346** pin (0.0402 5% resistor).
- The **I2C1\_SCL\_TP\_R** pin is connected to the **RZ347** pin (0.0402 5% resistor).

**I2C From CPU:**

- The **I2C1\_SDA\_TP\_R** pin is connected to the **RZ26** pin (0.0402 5% resistor).
- The **I2C1\_SCL\_TP\_R** pin is connected to the **RZ28** pin (0.0402 5% resistor).

**Touch Pad:**

- The Touch Pad is connected to a **3.3V\_TP** supply via a **10k** pull-up resistor (**RZ217**).
- The Touch Pad is connected to the I2C bus via a **10k** pull-up resistor (**RZ21**) and a **2k** pull-down resistor (**RZ20**).

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## Keyboard


Document Number  
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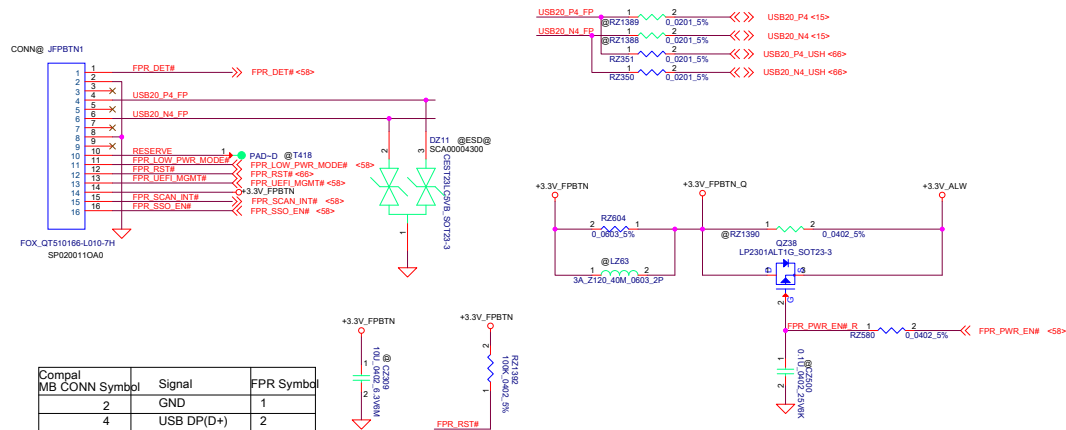
Reserve

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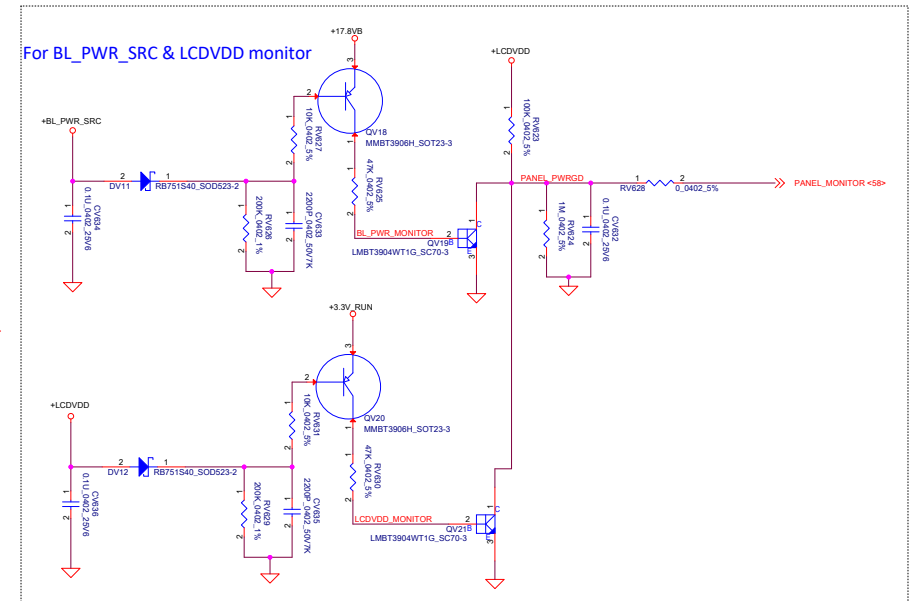
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Title					
Reserve for KB/TP/LED/LID					
Size	Document Number				Rev
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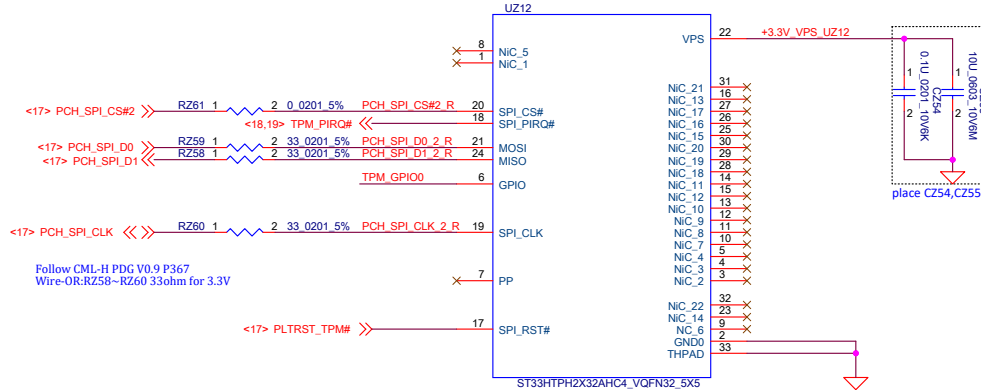
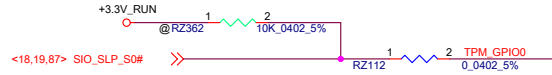
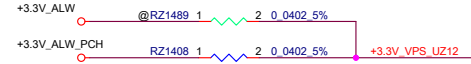
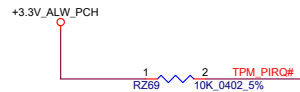
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FP in PWR BUTTON connector

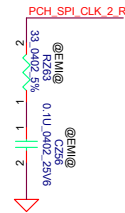


Compal MB CONN Symbol	Signal	FPR Symbol
2	GND	1
4	USB DP(D+)	2
6	USB DM(D-)	3
8	GND	4
10	RESERVED	5
12	FP RESET#	6
14	+3.3V_FPBTN	7
16	FPR_SSO_EN#	8
15	FPR_SCAN_INT#	9
13	FPR_UEFI_MGMT#	10
11	FPR_LOW_PWR_MODE#	11
9	NA	12
7	NA	13
5	NA	14
3	NA	15
1	FPR_DET(GND)	16

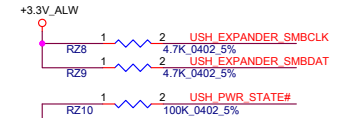
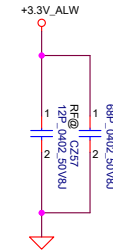
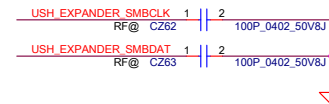
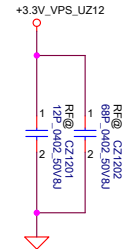




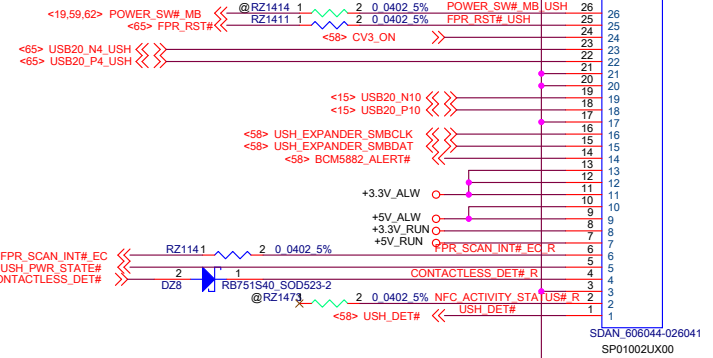
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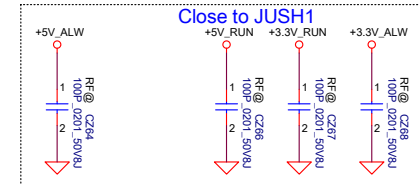
Close to UZ12



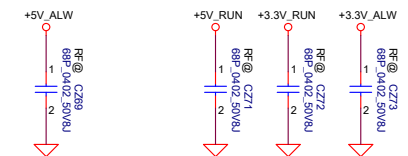
USH CONN



Use HRS\_TF31C-26S-0P5SH-800 footprint



Close to JUSH1

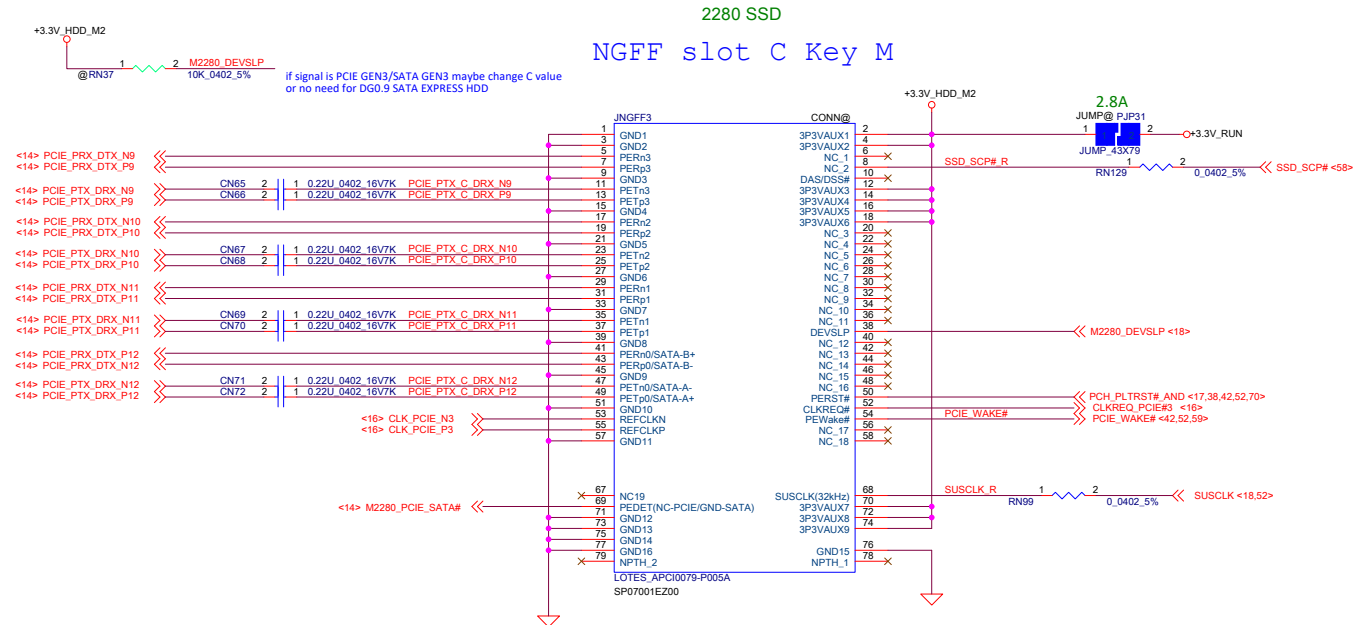
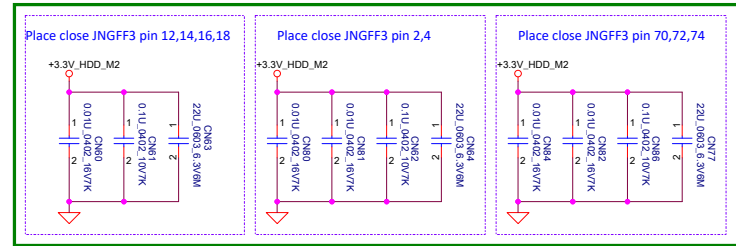


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				Size B	Document Number LA-J272P	Rev 0.2
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# Add Power Decoupling for support Intel Teton Glacier

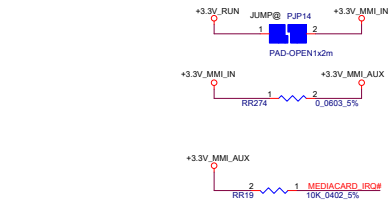


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Deciphered Date				2020/01/01				M2 2280 Socket			
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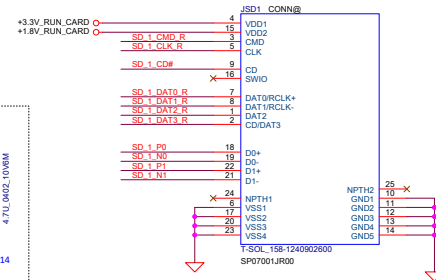
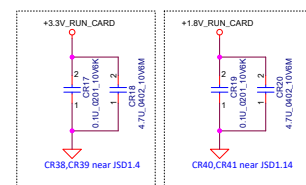
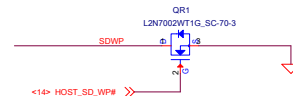
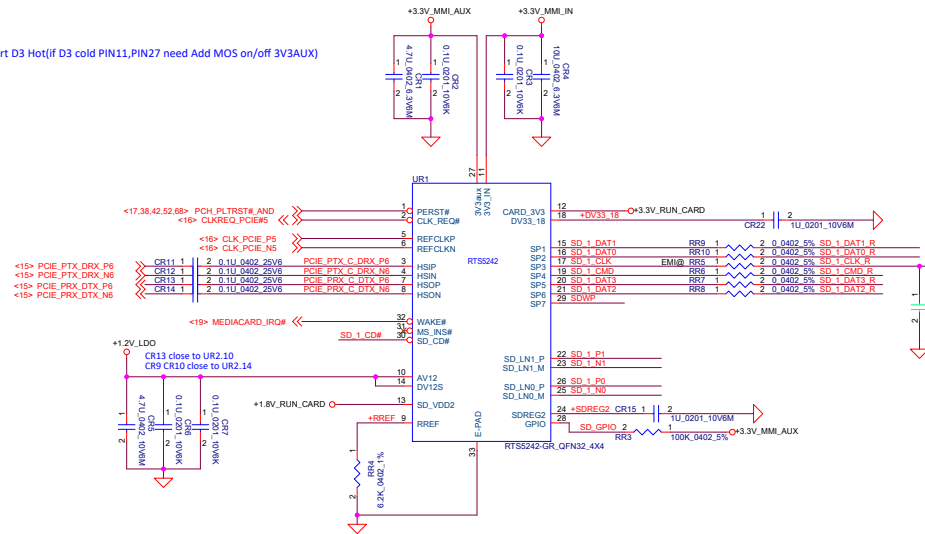
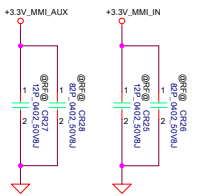
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eMMC / UFS		
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support D3 Hot(if D3 cold PIN11,PIN27 need Add MOS on/off 3V3AUX)



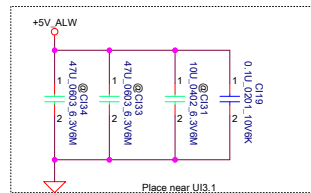
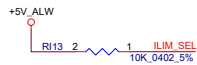
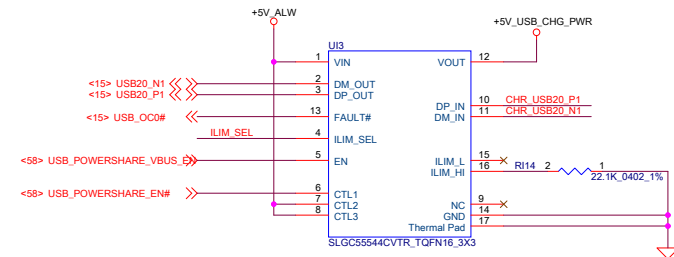
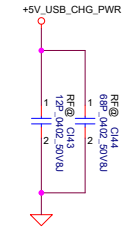
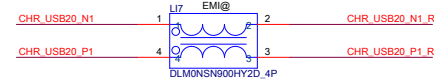
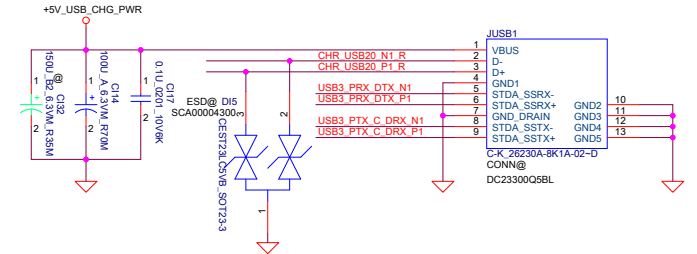
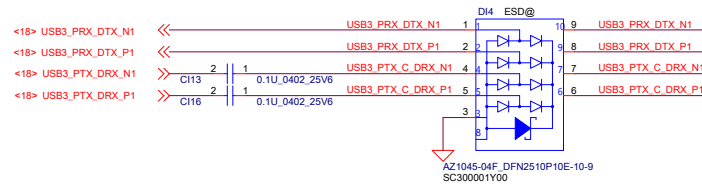
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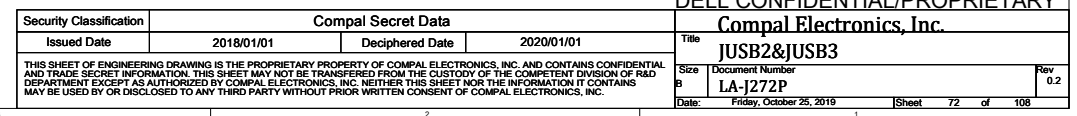
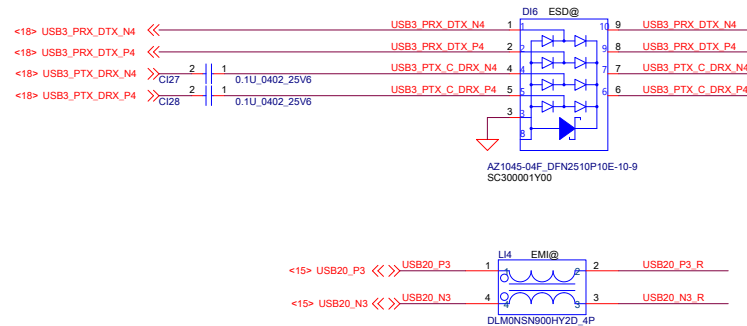
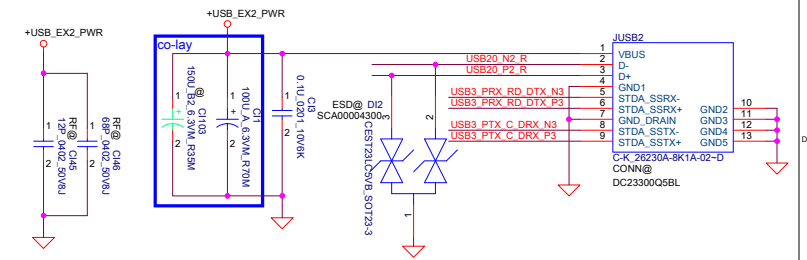
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Card Reader

# For PWR SW + Charger combine IC

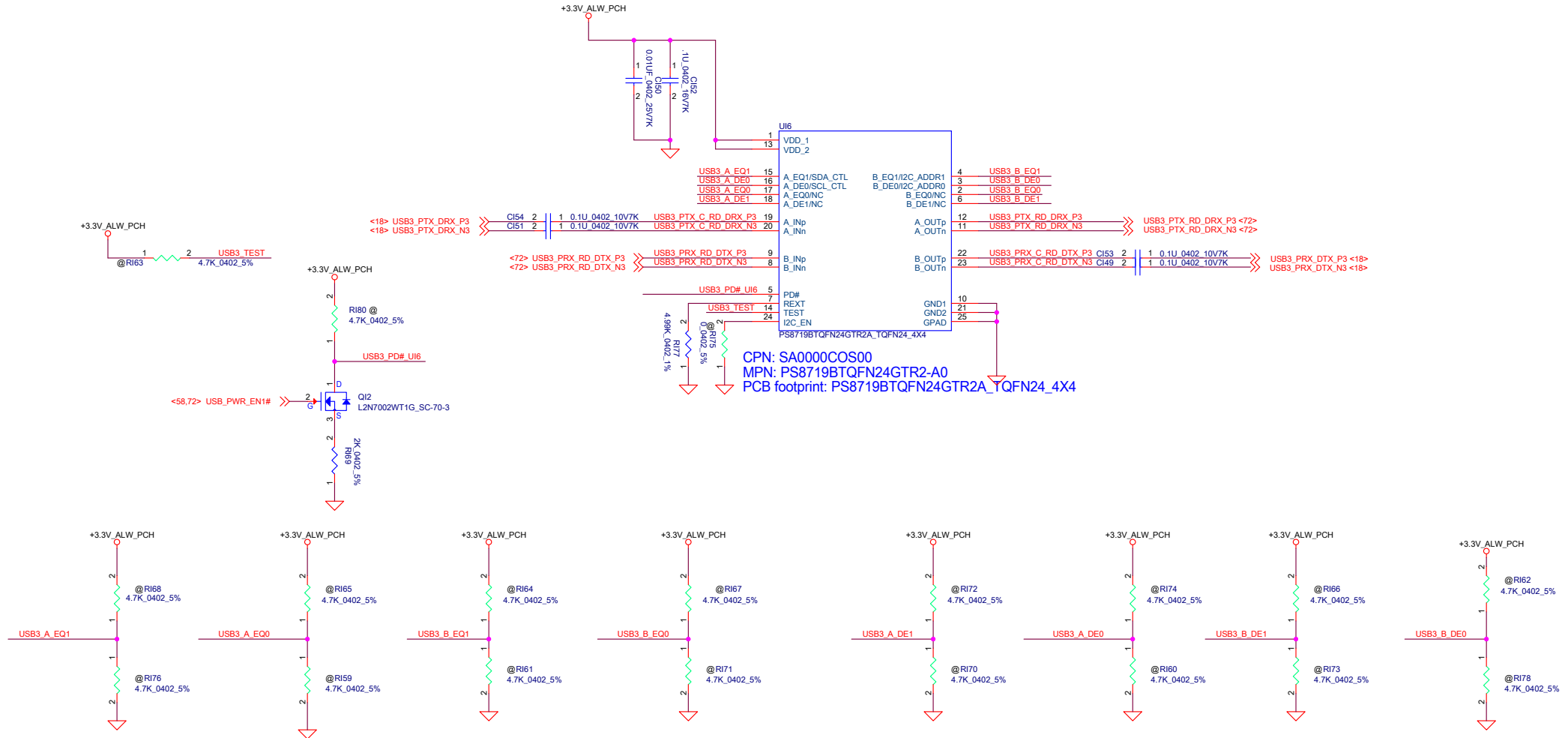


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Rev				0.2							



USB3 repeater from PS8713B change to PS8719B

FOR LEFT JUSB2 USE



Parade\_PS8719B

A_EQ1	A_EQ0	B_EQ1	B_EQ0	Recommended EQ
0	0	0	0	loss up to 9.5dB
0	1	0	1	loss up to 13dB
1	0	1	0	loss up to 4.5dB
1	1	1	1	loss up to 7.5dB

Both A\_EQ&B\_EQ have internal pull-down 150k

A_DE1	A_DE0	B_DE1	B_DE0	Recommended DE
0	0	0	0	3.5dB de-emphasis
0	1	0	1	No de-emphasis
1	0	1	0	2.7dB de-emphasis
1	1	1	1	5dB de-emphasis


Both A\_DE&B\_DE have internal pull-down 150k

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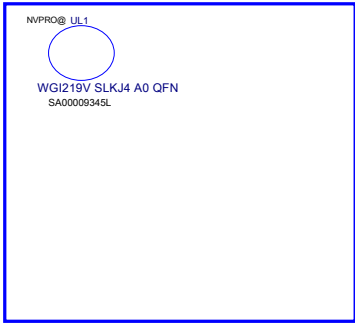
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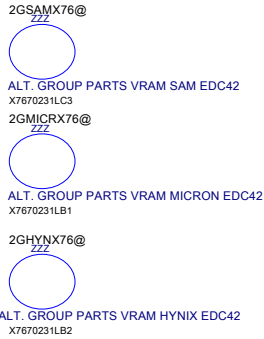
FOR NVPRO LAN chip BOM OPTION



FOR 14HD VRAM BOM OPTION

VENDER	STRAP	Part Number		Strap2,Strap1,Strap0 )		H:RV239 L:RV240	H:RV237 L:RV238	H:RV235 L:RV236	
Samsung	0x3	K4G80325FC-HC25 SA00009TA3L	2GSAM@ UV17  K4G80325FC-HC25	2GSAM@ UV18  K4G80325FC-HC25	( L, H, H )	2GSAM@ RV240  100K_0402_5%	2GSAM@ RV237  100K_0402_5%	2GSAM@ RV235  100K_0402_5%	
Micron	0x9	MT51J256M32HF-80:B SA00009T13L	2GMICR@ UV17  MT51J256M32HF-80:B	2GMICR@ UV18  MT51J256M32HF-80:B	( L, <span style="border: 1px solid black; padding: 0 2px;">M</span> , L )	2GMICR@ RV240  100K_0402_5%	2GMICR@ RV237  100K_0402_5%	2GMICR@ RV238  100K_0402_5%	2GMICR@ RV236  100K_0402_5%
Hynix	0xA	H5GC8H24AJR-R2C SA0000C171L	2GHYN@ UV17  H5GC8H24AJR-R2C	2GHYN@ UV18  H5GC8H24AJR-R2C	( L, <span style="border: 1px solid black; padding: 0 2px;">M</span> , H )	2GHYN@ RV240  100K_0402_5%	2GHYN@ RV237  100K_0402_5%	2GHYN@ RV238  100K_0402_5%	2GHYN@ RV235  100K_0402_5%

FOR 14HD VRAM X76



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Google Debug & INAs			
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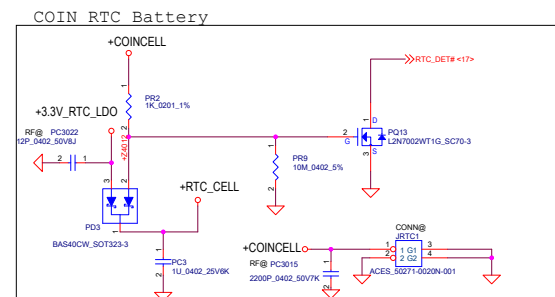


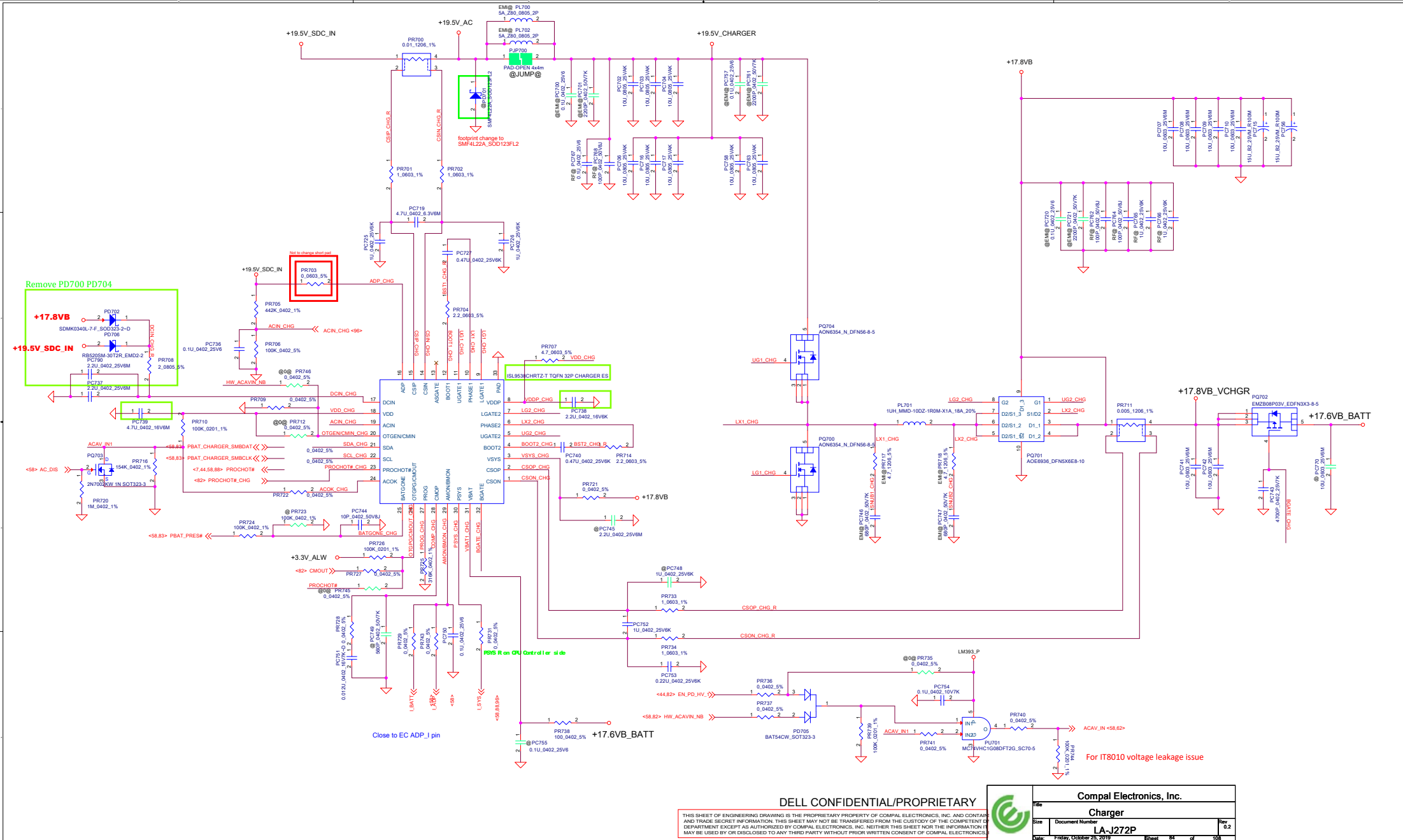
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Charger

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Layout to be clean  
PHZ1 close to SA choke  
PHZ1.1, PRZ3.2, PRZ4.2 differential to IC

TSMB0224J4702RE  
7.2329K0105C  
R15/0.9m  
R47/6.2m

Place close to Choke in VCCSA first phase circuit

PR1199 NA, need confirm

place close VR side

keep out with dirty net > 100 mil

keep out with dirty net > 100 mil

Place close to Choke in VCORE first phase circuit

keep out with dirty net > 100 mil

CFL-H82 (45W)  
IA: TDC=125A, Icc Max=165A, loadline=1.1mohm  
GT: TDC=25A, Icc Max=32A, loadline=2.7mohm  
SA: TDC=10A, Icc Max=11.1A, loadline=10.3mohm

CFL-H62 (45W)  
IA: TDC= 80A, Icc Max=128 A

CFL-H42 (45W)  
IA: TDC= 60A, Icc Max= 86A,

OCp  
IA@H82@H62: 201 A  
IA@H42: 137 A  
GT: 48A  
SA: 19.2A  
OVP  
DAC<370mV

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CPU\_CORE

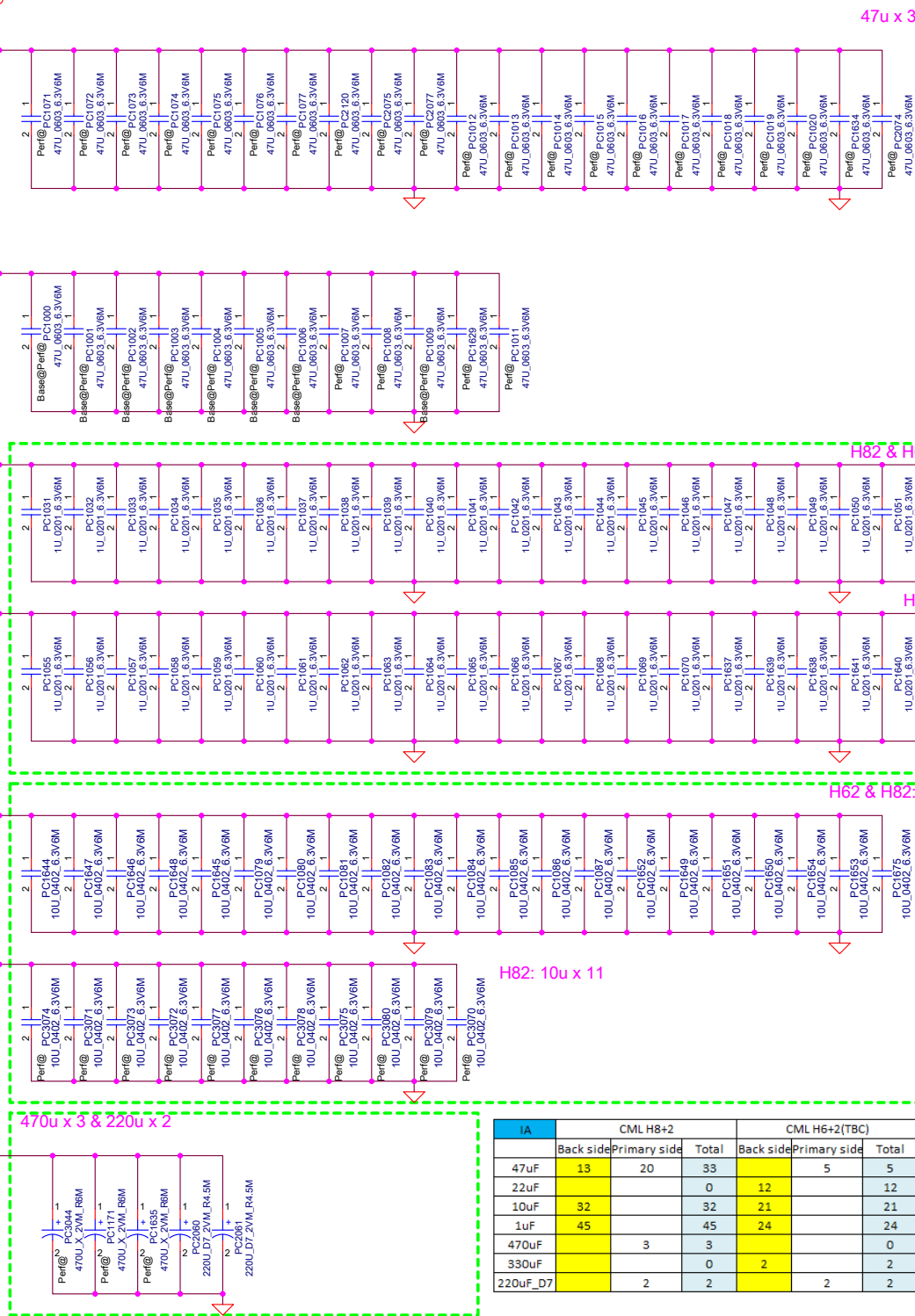
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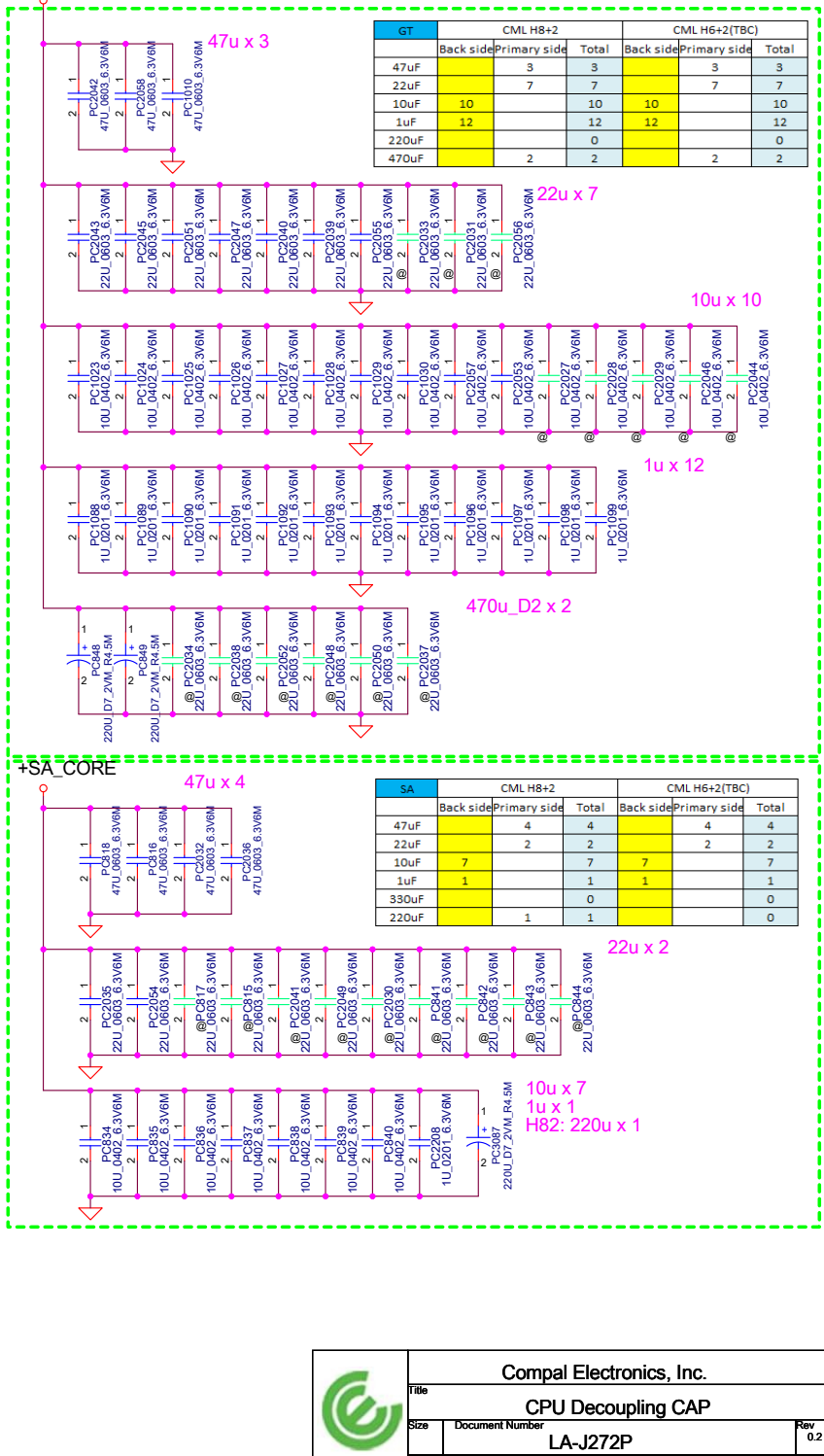
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## +IA\_CORE



## +GT\_CORE



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Operation phase Number	PSI Voltage setting
1 phase with DEM	0V to 0.4V
1 phase with CCM	0.8V to 1V
Active phase with CCM	1.4V to 5.5V

PSM VID and Output voltage control

- 1.Boot mode
- 2.Standby mode (don't support)
- 3.Normal mode

Pin connections:

- DSC@ PR1301: 1K, 0402, 5% to +3.3V\_RUN
- DSC@ PR1302: 0.0402, 5% to GPU\_PWM\_VID <27>
- DSC@ PR1303: 20.5K, 0402, 1% to +3.3V\_RUN
- DSC@ PR1305: 0.0402, 5% to NVVD0\_PSI <27>
- N18: 1.8V to +3.3V\_RUN
- Capacitor: 0.1uF, 0402, 25V6 to +3.3V\_RUN

14HD: N17S-G1 ( GB2C-64)  
15HD: N17S-G1-B (GB4C-128)  
15HP:N19M-Q3

**+17.8VB\_GPU**

**+GPU\_CORE**

**+5V\_UN**

**Switching frequency setting:**  
 $F_{sw} = (V_{in} - 0.5) / (2 \cdot V_{in} \cdot R_{ton} \cdot 3.2p) = 400KHz$

**RT8813DQGW\_WQFN24\_4X4**

**Place close HW side RH373**

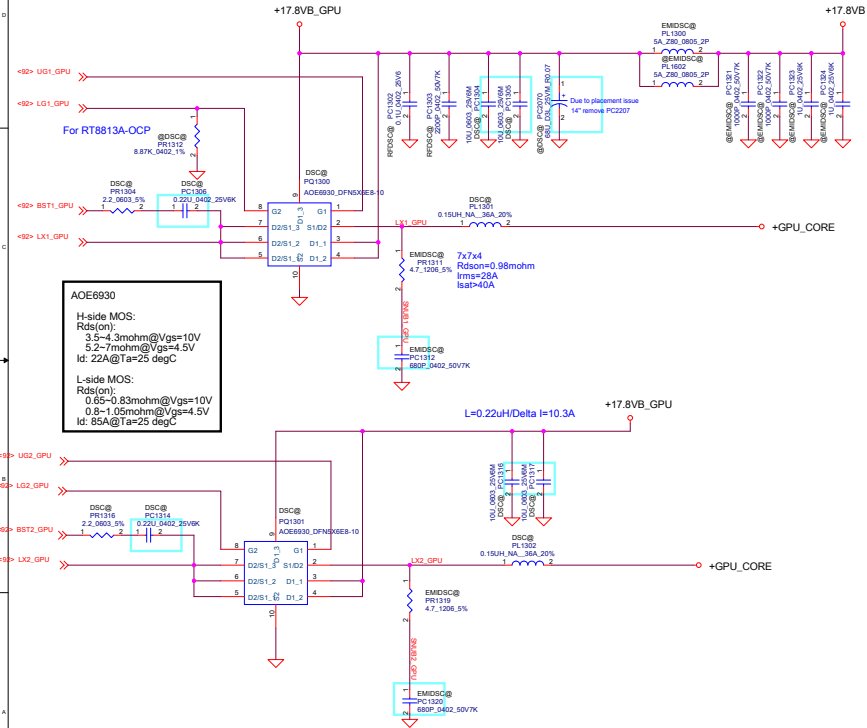
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GPU_CORE			
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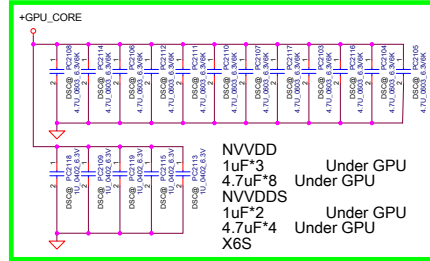
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+VGA\_CORE(N18M-Q3)  
TDC=30 A  
Peak 64 A (NVDD=54A, NVDDS=10A)  
OCPr=78.8 A

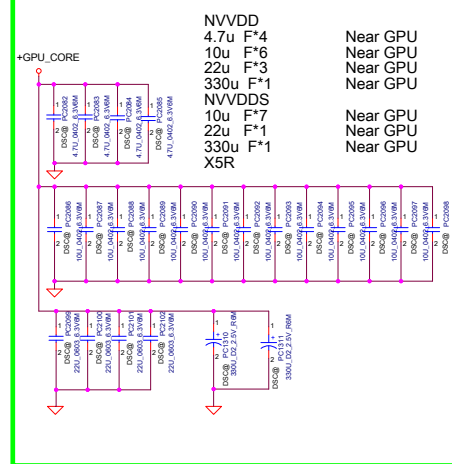
C=1\*330uF (6mohm)=330uF  
Vripple=Iripple\*ESR(min)=12.78A\*6mohm=76.69mV



#### Under GPU



#### Near GPU



power rail	cap[uf]	15HD		14HD	
		Under	Near	Under	Near
NVDD	1	8		3	
	4.7	16		8	4
	10		9		6
	22		7		3
NVDDS	330		1		1
	1	5		2	
	4.7			4	
	10	5	2		7
Total		798.2		958.2	

N18M-Q3-A1(GB4c-128)  
NVDD  
1uF\*5 Under GPU  
4.7uF\*16 Under GPU  
10uF\*8 Near GPU  
22uF\*7 Near GPU  
330uF\*1 Near GPU  
NVDDS  
1uF\*5 Under GPU  
10uF\*5 Under GPU  
10uF\*2 Near GPU  
22uF\*3 Near GPU

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Reserve

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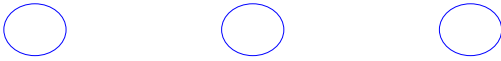
## CPU

H82@ PRZ84 25.5K\_0402\_1%  
H42@ PRZ68 82.5K\_0402\_1%  
H42@ PRZ48 15K\_0402\_1%  
H82@ PRZ68 130K\_0402\_1%  
H42@ PRZ47 28K\_0402\_1%  
H82@ PRZ32 2.74K\_0402\_1%



## CPU choke

H82@ PLH1 0.15UH\_MMD06DZER15MEM2L\_36A\_20%  
H82@ PLH2 0.15UH\_MMD06DZER15MEM2L\_36A\_20%  
H82@ PLH3 0.15UH\_MMD06DZER15MEM2L\_36A\_20%



H82@ PLH4 0.15UH\_MMD06DZER15MEM2L\_36A\_20%

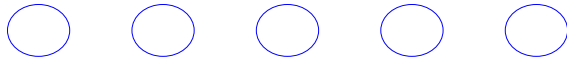


## OUTPUT CAPS

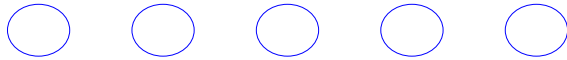
Base@ PC3090 220U\_D7\_2VM\_R4.5M  
Base@ PC3092 220U\_D7\_2VM\_R4.5M



Base@ PC3093 22U\_0603\_6.3V6M  
Base@ PC3091 22U\_0603\_6.3V6M  
Base@ PC3095 22U\_0603\_6.3V6M  
Base@ PC3094 22U\_0603\_6.3V6M  
Base@ PC3096 22U\_0603\_6.3V6M



Base@ PC3097 22U\_0603\_6.3V6M  
Base@ PC3098 22U\_0603\_6.3V6M  
Base@ PC3099 22U\_0603\_6.3V6M  
Base@ PC3100 22U\_0603\_6.3V6M  
Base@ PC3101 22U\_0603\_6.3V6M




Base@ PC3102 22U\_0603\_6.3V6M  
Base@ PC3104 22U\_0603\_6.3V6M  
Base@ PC3106 22U\_0603\_6.3V6M  
Base@ PC3107 22U\_0603\_6.3V6M  
Base@ PC3110 22U\_0603\_6.3V6M  
Base@ PC3113 22U\_0603\_6.3V6M



Base@ PC3103 22U\_0603\_6.3V6M  
Base@ PC3105 22U\_0603\_6.3V6M  
Base@ PC3109 22U\_0603\_6.3V6M  
Base@ PC3108 22U\_0603\_6.3V6M  
Base@ PC3111 22U\_0603\_6.3V6M  
Base@ PC3112 22U\_0603\_6.3V6M

GPU  
IC

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Layer No.	Name	Er	Material	Thickness (Material SPEC.) Unit : mil	Thickness (Actuality) Unit : mil	Delay Time (ps/inch)	DK	DF(1GHz)	35 ± 3.5 ohm single-end	40 ± 4 ohm single-end	42 ± 4.2 ohm single-end	45 ± 4.5 ohm single-end	50 ± 5 ohm single-end	80 ± 8 ohm Diff	85 ± 8.5 ohm Diff	88 ± 8.8 ohm Diff	90 ± 9 ohm Diff	100 ± 10 ohm Diff	REF	90 ± 9 ohm Diff	85 ± 8.5 ohm Diff	REF	100 ± 10 ohm Diff	REF
		3.7	SolderMask	GA-150LL	0.50		3.70	0.03	trace Width (±12%)	trace Width (±12%)	trace Width (±12%)	trace Width (±12%)	trace Width (±12%)	trace Width (±12%)	trace Width (±12%)	trace Width (±12%)	trace Width (±12%)	trace Width (±12%)		trace Width (±12%)	trace Width (±12%)		trace Width (±12%)	
			Add Plating		0.95																			
1	Top		Copper foil	0.5oz	0.65				8.5	8.6	8	5.3	4.3	5/4.5	4.2/4	3.9/4.1	4/5	3.5/7	L2	7.1/4	8.5/4	L3	10.5/4.5	No REF
2	GND/PWR	3.7	Prepreg	1086 or 1080	2.70	152.90	3.70	0.0195	34.7	40.3	42.48	45.36	50.26	80.67	85.22	88.24	90.62	100.84		90.66	85.15			
		3.7	Copper foil	0.5oz	0.65																			
3	Sig1		Core	3mil	3.00		3.70	0.0187																
		3.7	Copper foil	0.5oz	0.65				6	4.7	4.5	3.8	3.1	4/3.5	3.7/4	3.5/4.5	3.5/5.5	3/7.5	L2/L4				9/5	No REF
4	GND/PWR	3.8	Prepreg	2116	4.20	163.60	3.80	0.0176	34.78	40.33	41.35	45.37	50.27	80.24	85.03	88.78	90.8	100.14					99.19	
		3.7	Copper foil	0.5oz	0.65																			
5	Sig2		Core	3mil	3.00		3.70	0.0187																
		3.7	Copper foil	0.5oz	0.65				6	4.7	4.5	3.8	3.1	4/3.5	3.7/4	3.5/4.5	3.5/5.5	3/7.5	L4/L6				9/5.5	No REF
6	GND/PWR	3.8	Prepreg	2116	4.20	163.60	3.80	0.0176	34.78	40.33	41.35	45.37	50.27	80.24	85.03	88.78	90.8	100.14					10.16	
		3.7	Copper foil	0.5oz	0.65																			
7	Sig3		Core	3mil	3.00		3.70	0.0187																
		3.7	Copper foil	0.5oz	0.65				7.5	5.8	5.5	4.7	3.8	4.5/3.5	4.2/4	4/4.5	4/5	3.5/7.5	L6/L9				9/5.5	No REF
8	Sig4		Prepreg	2116	4.20	163.60	3.80	0.0176	34.48	40.3	41.55	45.29	50.47	80.59	85.13	88.67	90.14	100.62					99.88	
		3.7	Copper foil	0.5oz	0.65				7.5	5.8	5.5	4.7	3.8	4.5/3.5	4.2/4	4/4.5	4/5	3.5/7.5	L6/L9				9/5.5	No REF
9	GND/PWR		Core	3mil	3.00		3.70	0.0187																
		3.7	Copper foil	0.5oz	0.65																			
10	Sig5		Prepreg	2116	4.20	163.60	3.80	0.0176																
		3.7	Copper foil	0.5oz	0.65				6	4.7	4.5	3.8	3.1	4/3.5	3.7/4	3.5/4.5	3.5/5.5	3/7.5	L9/L11				9/5	No REF
11	GND/PWR	3.7	Core	3mil	3.00		3.70	0.0187	34.78	40.33	41.35	45.37	50.27	80.24	85.03	88.78	90.8	100.14					99.19	
		3.7	Copper foil	0.5oz	0.65																			
12	Bottom		Prepreg	1086 or 1080	2.70	152.90	3.70	0.0195																
		3.7	Copper foil	0.5oz	0.65				8.5	8.6	8	5.3	4.3	5/4.5	4.2/4	3.9/4.1	4/5	3.5/7	L11	7.1/4	8.5/4	L10	10.5/4.5	No REF
			Add Plating		0.95				34.7	40.3	42.48	45.36	50.26	80.67	85.22	88.24	90.62	100.84					99.63	
		3.7	SolderMask		0.50		3.70	0.03																
Overall Thickness (1.2mm ± 10%)					47.90000																			
Reference GCE RD data					1.21606																			

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Stack Up

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Segment	Tilne Type	Reference	Via Count	Max Length, mm	
				Segment	Total
BQ/M7	M5/SL	VSS	1	12.7	101.6
M1/M6	M5/SL/DSL	VSS	1	38.1	
M2/M5	M5	VSS	0	12.7	

[illegible]

13. Minimum length for M1, M4 and M6: 12.7mm  
14. Minimum length for M2, M3 and M5: 2.54mm  
15. SPI branches of segment M3+M4 need to have length matching of 2.54mm  
16. Length matching between CLK and DATA/CS# signals: 12.7mm  
17. Trace spacing between DATA and DATA signals: 0.250mm  
18. Trace spacing between CLK and DATA/Other signals: 0.375mm

The diagram illustrates the SPI interface connections between three main components: the CPU, the EC (Embedded Controller), and the WSON8 Flash ROM.

**CPU Connections:**

- SPI0\_CLK:** Connected to PCH\_SPL\_CLK\_PCH (0ohm) and PCH\_SPL\_CLK.
- SPI0\_IO[0:1]:** Connected to PCH\_SPL\_D[0:1]\_PCH (0ohm) and PCH\_SPL\_D[0:1].
- SPI0\_IO[2:3]:** Connected to PCH\_SPL\_D[2:3]\_PCH (0ohm) and PCH\_SPL\_D[2:3].
- SPI0\_CS#:** Connected to PCH\_SPL\_CS#0 (green line) and PCH\_SPL\_CS#2 (purple line).

**EC Connections:**

- SHD\_CLK:** Connected to SHD\_CLK (33ohm) and PCH\_SPL\_CLK.
- SHD\_IO[0:1]:** Connected to SHD\_IO[0:1] (33ohm) and PCH\_SPL\_D[0:1].
- SHD\_IO[2:3]:** Connected to SHD\_IO[2:3] (75ohm) and PCH\_SPL\_D[2:3].
- SHD\_CS#0:** Connected to SHD\_CS#0 (green line) and PCH\_SPL\_CS#0.

**WSON8 Flash ROM Connections:**

- SPI\_CLK:** Connected to PCH\_SPL\_CLK\_0\_R (33ohm).
- SPI\_IO[0:1]:** Connected to PCH\_SPL\_D[0:1]\_0\_R (33ohm).
- SPI\_IO[2:3]:** Connected to PCH\_SPL\_D[2:3]\_0\_R (22ohm).
- CS#:** Connected to SPI\_CS#0\_R (0ohm) and PCH\_SPL\_CS#2\_R (purple line).

**Additional Connections and Components:**


- +3.3V\_SPI:** A 1.7k resistor is connected to the SPI lines.
- 1Kohm Resistors:** Two 1Kohm resistors are connected to the PCH\_SPL\_D2\_PCH and PCH\_SPL\_D0\_PCH lines.
- 33ohm Resistors:** Multiple 33ohm resistors are connected to the SPI lines at various points.
- 75ohm Resistor:** A 75ohm resistor is connected to the SHD\_IO[2:3] line.
- 0ohm Resistors:** Several 0ohm resistors are used as jumpers for the SPI lines.
- UC5 System ROM part:** A 32MB WSON8 Flash ROM is connected to the SPI lines.
- UE12 TPM ST33HPTH2032AHC1:** A TPM device is connected to the SPI lines.
- JXDP1:** A JXDP1 component is connected to the SPI lines.



Version Change List (P. I. R. List)					Solution		Rev.
Item	Page#	Date	Issue	Description	Description		
1	38	2019/9/20		Reserve RC delay on +LCDVDD enable for LCD sequence adjustment flexibility(X11 platform)	add RV180 SD028000080(S RES 1/16W 0 +-5% 0402) and CV80(non-pop) SE000000K80(S CER CAP 1U 6.3V K X5R 0402) on DV3.1	0.2(X01)	
2	19 38	2019/9/20		Spyglass lesson learn, reserve PCH GPIO for TS_RST# control(X11 platform)	P19 add net TS_RST# on UH1.BE17(GPP_D13) with offpage P38 add two control path RZ311(SD028000080(S RES 1/16W 0 +-5% 0402, pop) & RZ310(SD028000080(S RES 1/16W 0 +-5% 0402, no-pop)on JIRTS1.1(TS_RST#_R) by PCH & EC(PCH_PLTRST#_AND) respectively,	0.2(X01)	
3	52	2019/10/9		CML-H not light up LCD with AX201 installed, implement new push-pull and-gate as level shift for CNVi RF_RESET & CLKREQ_CNV(Aligned with Rialto and Fiorano, X11 platform)	add UZ1,UZ63 SA00003R000(S IC NL17SZ08DFT2G SC70 5P AND GATE) between PCH & WLAN NGFF	0.2(X01)	
4	52 58	2019/10/9		Dell request BT_RADIO_DIS# controlled by both EC & PCH(X11 platform)	P52 add two control path DZ16,DZ2 SCS00003700(S SCH DIO RB751S40 SOD523) on JNGFF1.54 BT_RADIO_DIS# by both PCH & WLAN NGFF P58 change RE11 SD028100380(S RES 1/16W 100K +-5% 0402) form no-pop to pop	0.2(X01)	
5	59	2019/10/9		DVT1.0 PCB revision, Board_ID change to X01 (X11 platform)	change RE79 from SD000001B80(S RES 1/16W 240K +-1% 0402) to SD034130380(S RES 1/16W 130K +-1% 0402)	0.2(X01)	
6	17	2019/10/15		MEC5107 D4 ver has fixed load code issue, depop WDT circuit(X11 platform)	change QZ9,RZ663,CZ622 from pop to no-pop	0.2(X01)	
7	44	2019/10/15		1) Dell PW SA request to disconnect PD PROHOT# control (X11 platform) 2) TI request, for TypeC disable feature(X11 platform)	1) change RT85 (SD028000080(S RES 1/16W 0 +-5% 0402, pop) from pop to no-pop(X11 platform) 2) change RT79 (SD028000080(S RES 1/16W 0 +-5% 0402, pop) from no-pop to pop(X11 platform)	0.2(X01)	
8	14	2019/10/15		MLCC reduction for baseline sku	add net IA_BASELINE_SEL# on UH1.N48(GPP_K4), and PU/PD RES R105,R106 SD028100280(S RES 1/16W 10K +-5% 0402), PU stands for baseline sku	0.2(X01)	
9							

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